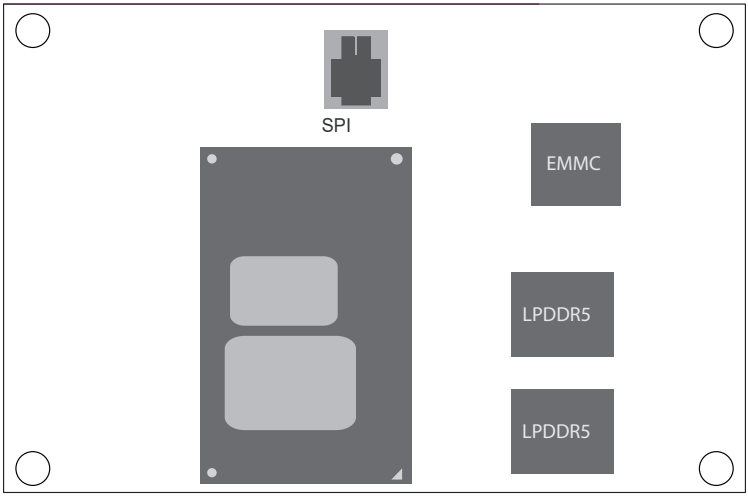
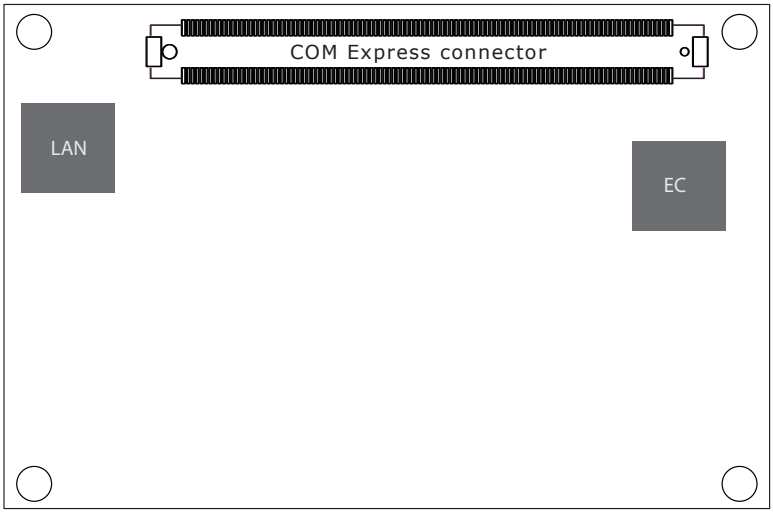
## Board Layout and COM Express Pin Assignments

### TOP




### BOTTOM



## ▶ COM Express Pin Assignments

### Pin List for Pin-Out Type 10

The table below is a comprehensive list of all signal pins supported on the single 220-pin COM Express connectors as defined for Type 10 in the PICMG COM.0 R3.0 specification.

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 1 | GND (FIXED) | | GND (FIXED) | |
| 2 | GBE0_MDI3- | | GBE0_ACT# | |
| 3 | GBE0_MDI3+ | | LPC_FRAME# | |
| 4 | GBE0_LINK100# | GBE1_LED1000# | LPC_AD0 | |
| 5 | GBE0_LINK1000# | GBE1_LED2500# | LPC_AD1 | |
| 6 | GBE0_MDI2- | | LPC_AD2 | |
| 7 | GBE0_MDI2+ | | LPC_AD3 | |
| 8 | GBE0_LINK# | | LPC_DRQ0# | PU 10K to 3.3V |
| 9 | GBE0_MDI1- | | LPC_DRQ1# | PU 10K to 3.3V |
| 10 | GBE0_MDI1+ | | LPC_CLK | |
| 11 | GND (FIXED) | | GND (FIXED) | |
| 12 | GBE0_MDI0- | | PWRBTN# | |
| 13 | GBE0_MDI0+ | | SMB_CK | |
| 14 | GBE0_CTREF | NC | SMB_DAT | |
| 15 | SUS_S3# | | SMB_ALERT# | |
| 16 | SATA0_TX+ | | SATA1_TX+ | |
| 17 | SATA0_TX- | | SATA1_TX- | |
| 18 | SUS_S4# | | SUS_STAT# | NC |
| 19 | SATA0_RX+ | | SATA1_RX+ | |
| 20 | SATA0_RX- | | SATA1_RX- | |
| 21 | GND (FIXED) | | GND (FIXED) | |
| 22 | USB_SSRX0- | | USB_SSTX0- | |
| 23 | USB_SSRX0+ | | USB_SSTX0+ | |
| 24 | SUS_S5# | | PWR_OK | |
| 25 | USB_SSRX1- | | USB_SSTX1- | |
| 26 | USB_SSRX1+ | | USB_SSTX1+ | |

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 27 | BATLOW# | | WDT | |
| 28 | (S)ATA_ACT# | | HDA_SDN2/SNDW0_CLK** | |
| 29 | HDA_SYNC | | HDA_SDIN1/SNDW0_DAT** | |
| 30 | HDA_RST# | | HDA_SDIN0 | |
| 31 | GND (FIXED) | | GND (FIXED) | |
| 32 | HDA_BITCLK | | SPKR | |
| 33 | HDA_SDOUT | | I2C_CK | |
| 34 | BIOS_DIS0# | | I2C_DAT | |
| 35 | THRMTRIP# | | THRM# | |
| 36 | USB6- | | USB7- | |
| 37 | USB6+ | | USB7+ | |
| 38 | USB_6_7_OC# | | USB_4_5_OC# | |
| 39 | USB4- | | USB5- | |
| 40 | USB4+ | | USB5+ | |
| 41 | GND (FIXED) | | GND (FIXED) | |
| 42 | USB2- | | USB3- | |
| 43 | USB2+ | | USB3+ | |
| 44 | USB_2_3_OC# | | USB_0_1_OC# | |
| 45 | USB0- | | USB1- | |
| 46 | USB0+ | | USB1+ | |
| 47 | VCC_RTC | | ESPI_EN# | NC |
| 48 | RSVD | | USB0_HOST_PRSNT | NC |
| 49 | GBE0_SDP | | SYS_RESET# | |
| 50 | LPC_SERIRQ | | CB_RESET# | |
| 51 | GND (FIXED) | | GND (FIXED) | |
| 52 | RSVD | CLKOUT_PCIE2_P_BTB | RSVD | PCIE_CLK_REQ1_BTB# |
| 53 | RSVD | CLKOUT_PCIE2_N_BTB | RSVD | NC |
| 54 | GPI0 | | GPO1 | |
| 55 | GP_SPI_CS# | | GP_SPI_MISO | NC |
| 56 | GP_SPI_CK | | GP_SPI_MOSI | NC |

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 57 | GND | | GPO2 | |
| 58 | PCIE_TX3+ | | PCIE_RX3+ | |
| 59 | PCIE_TX3- | | PCIE_RX3- | |
| 60 | GND (FIXED) | | GND (FIXED) | |
| 61 | PCIE_TX2+ | | PCIE_RX2+ | |
| 62 | PCIE_TX2- | | PCIE_RX2- | |
| 63 | GPI1 | | GPO3 | |
| 64 | PCIE_TX1+ | | PCIE_RX1+ | |
| 65 | PCIE_TX1- | | PCIE_RX1- | |
| 66 | GND | | WAKE0# | |
| 67 | GPI2 | | WAKE1# | |
| 68 | PCIE_TX0+ | | PCIE_RX0+ | |
| 69 | PCIE_TX0- | | PCIE_RX0- | |
| 70 | GND (FIXED) | | GND (FIXED) | |
| 71 | LVDS_A0+/eDP_TX2+** | | DDI0_PAIR0+ | |
| 72 | LVDS_A0-/eDP_TX2-** | | DDI0_PAIR0- | |
| 73 | LVDS_A1+/eDP_TX1+** | | DDI0_PAIR1+ | |
| 74 | LVDS_A1-/eDP_TX1-** | | DDI0_PAIR1- | |
| 75 | LVDS_A2+/eDP_TX0+** | | DDI0_PAIR2+ | |
| 76 | LVDS_A2-/eDP_TX0-** | | DDI0_PAIR2- | |
| 77 | LVDS_VDD_EN/ eDP_VDD_EN** | | DDI0_PAIR4+ | NC |
| 78 | LVDS_A3+ | | DDI0_PAIR4- | NC |
| 79 | LVDS_A3- | | LVDS_BKLT_EN/ eDP_BKLT_EN** | |
| 80 | GND (FIXED) | | GND (FIXED) | |
| 81 | LVDS_A_CK+/ eDP_TX3+** | | DDI0_PAIR3+ | |
| 82 | LVDS_A_CK-/ eDP_TX3-** | | DDI0_PAIR3- | |
| 83 | LVDS_I2C_CK/ eDP_AUX+** | | LVDS_BKLT_TRL/ eDP_BKLT_CTRL** | |
| 84 | LVDS_I2C_DAT/ eDP_AUX-** | | VCC_5V_SBY | |
| 85 | GPI3 | | VCC_5V_SBY | |
| 86 | RSVD | | VCC_5V_SBY | |
| 87 | eDP_HPD** | | VCC_5V_SBY | |
| 88 | PCIE_CLK_REF+ | | BIOS_DIS1# | |

| Pin | Row A | "ASL9A2 Difference" | Row B | "ASL9A2 Difference" |
|---|---|---|---|---|
| 89 | PCIE_CLK_REF- | | DDI0_HPD | |
| 90 | GND(FIXED) | | GND(FIXED) | |
| 91 | SPI_POWER | | DDI0_PAIR5+ | NC |
| 92 | SPI_MISO | | DDI0_PAIR5- | NC |
| 93 | GPO0 | | DDI0_PAIR6+ | NC |
| 94 | SPI_CLK | | DDI0_PAIR6- | NC |
| 95 | SPI_MOSI | | DDI0_DDC_AUX_SEL | |
| 96 | TPM_PP | | USB7_HOST_PRSNT | NC |
| 97 | TYPE10# | | SPI_CS# | |
| 98 | SER0_TX | | DDI0_CTRLCLK_AUX+ | |
| 99 | SER0_RX | | DDI0_CTRLDATA_AUX- | |
| 100 | GND (FIXED) | | GND (FIXED) | |
| 101 | SER1_TX | | FAN_PWMOUT | |
| 102 | SER1_RX | | FAN_TACHIN | |
| 103 | LID# | | SLEEP# | |
| 104 | VCC_12V | | VCC_12V | |
| 105 | VCC_12V | | VCC_12V | |
| 106 | VCC_12V | | VCC_12V | |
| 107 | VCC_12V | | VCC_12V | |
| 108 | VCC_12V | | VCC_12V | |
| 109 | VCC_12V | | VCC_12V | |
| 110 | GND(FIXED) | | GND(FIXED) | |

Note:

1. ** eDP (in place of LVDS) is BOM option supported by project basis.
2. ** SNDW (in place of HDA) is BOM option supported by project basis.
3. ASL9A2 (Mini module) allows wide range input voltage wtih 4.75V to 20V from VCC_12V power pins.
4. For PCIe device down components on the carrier board, please use and place on the PCIe Lane0 port first.

DFI reserves the right to change the specifications at any time prior to the product's release. This QR may be based on the product's revision. For more documentation and drivers, please visit the download page at www.dfi.com/downloadcenter, or via the QR codes to the right.