DFI

EHL701

Intel Atom® Processor (Qseven)

User's Manual

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Changes after the publication's first release will be based on the product's revision. The website will always provide the most updated information.

Trademarks

Product names or trademarks appearing in this manual are for identification purpose only and are the properties of the respective owners.

Qseven Specification Reference

Qseven Specification Reference Specification,
please refer to: http://www.qseven-standard.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- Wear an antistatic wrist strap.
- Do all preparation work on a static-free surface.
- Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

The accessories in the package may not come similar to the information listed below. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- EHL701 Board
- Cooler

Optional Items

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

- Qseven Carrier Board
- Heat Spreader

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

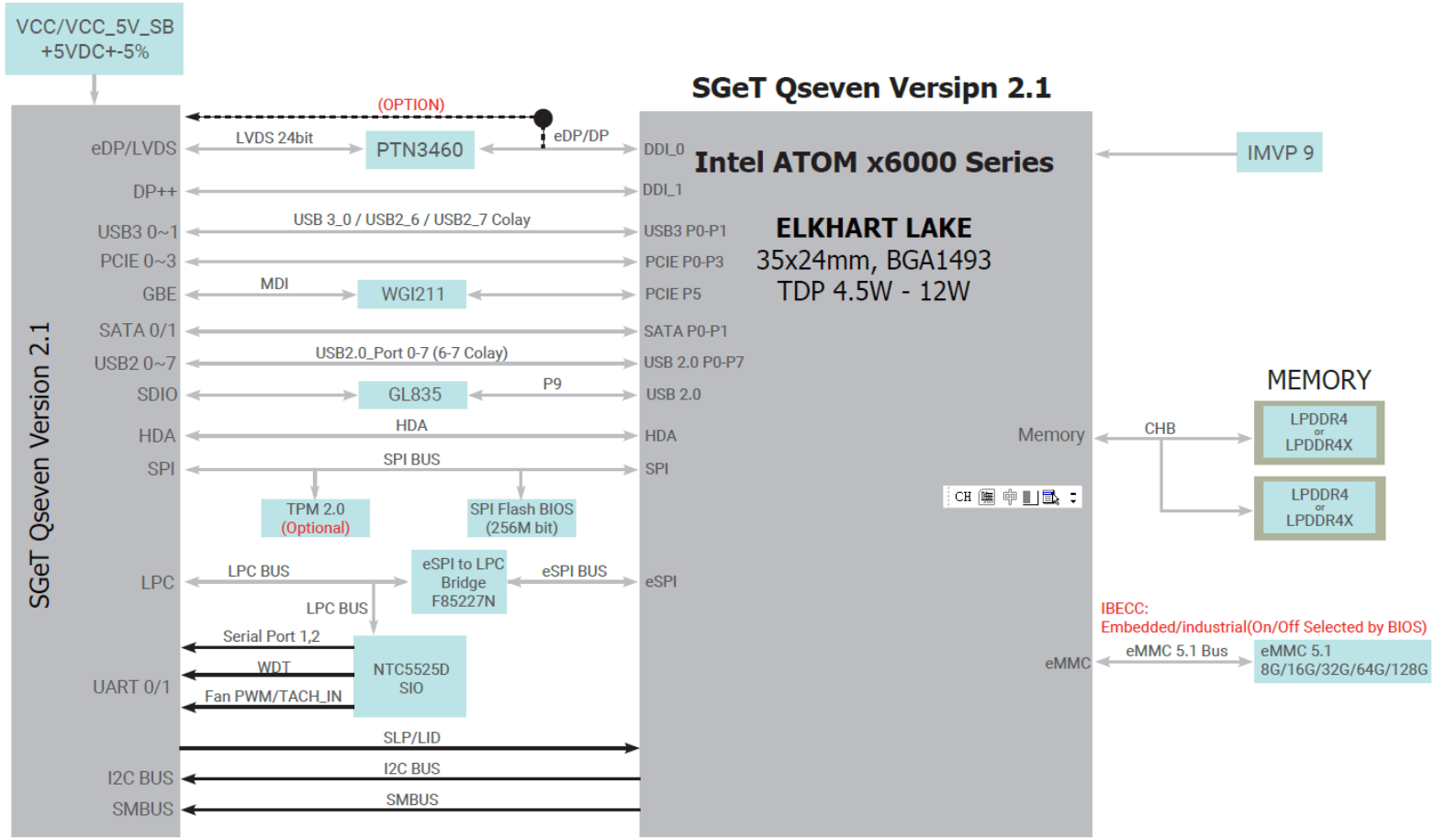
Chapter 1 - Introduction

▶ Specification

SYSTEM	Processor	Intel Atom® x6000 Series Processors Intel Pentium® N and J Series Processors Intel Celeron® N and J Series Processors
	Memory	4GB/8GB/16GB LPDDR4 Memory Down Dual Channel LPDDR4 3200MHz
	BIOS	AMI SPI 256Mbit (supports UEFI boot only)
GRAPHICS	Controller	Intel® HD Graphics Gen9LP Series
	Feature	OpenGL 5.0, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H.265, VP8, VP9, MVC HW Encode: AVC/H.264, JPEG/MJPEG, HEVC/H.265, VP8, VP9, MVC
	Display	1 x DDI (HDMI/DVI/DP++) 1 x eDP/LVDS HDMI: resolution up to 3840x2160 @ 30Hz DP++: resolution up to 4096x2160 @ 60Hz eDP: resolution up to 3840x2160 @ 60Hz
	Dual Displays	eDP/LVDS + DDI
EXPANSION	Interface	4 x PCIe x1 (Gen 2) 1 x SDIO 1 x LPC 1 x I2C 1 x SMBus 1 x SPI 1 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel I211
I/O	USB	1 x USB 3.1 + 8 x USB 2.0 / 2 x USB3.1 + 6 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s)
	eMMC	Supports up to 128GB eMMC, NC as default eMMC 5.1, BGA-153 Ball 8~128G(MLC mode)
	GPIO	1 x 4-bit GPIO
WATCHDOG TIMER	Output & Interval	Output & Interval
SECURITY	TPM	dTPM or fTPM (Optional)
Power	Type	5V, 5VSB, VCC_RTC
	Consumption	Typical: x6212RE: 12V @ 0.98A (11.76W) Max.: x6212RE:12V @ 1.45A (17.4W)

OS SUPPORT (UEFI ONLY)	Microsoft	Windows 10 IoT Enterprise 64-bit
	Linux	Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C, -40 to 85°C , -5 to 65°C(opt.) Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH
	MTBF	773,944 hrs @ 25°C; 335,063 hrs @ 45°C; 138,841 hrs @ 60°C; 29,888 hrs @ 85°C
MECHANICAL	Dimensions	Qseven Form Factor 70mm (2.76") x 70mm (2.76")
	Compliance	Qseven Specification Revision 2.1
STANDARDS AND CERTIFICATIONS	Certification	CE, FCC Class B, RoHS, UKCA

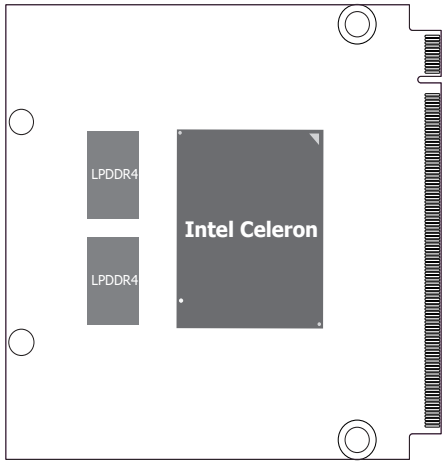
▶ Block Diagram



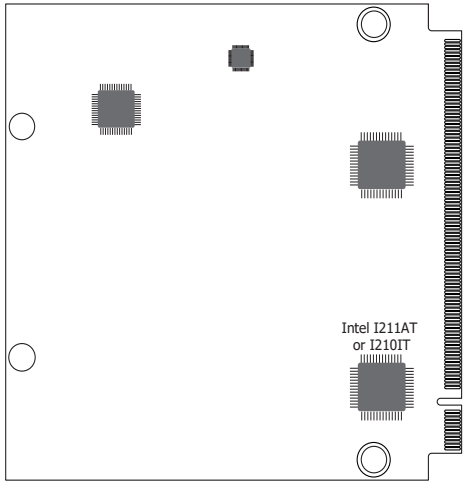
Chapter 2 - Hardware Installation

▶ Board Layout

TOP VIEW



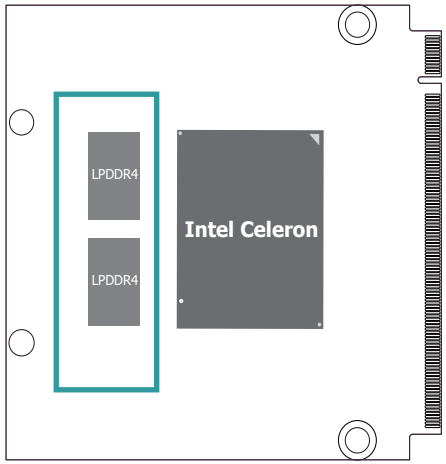
BOTTOM VIEW



Important:
Boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

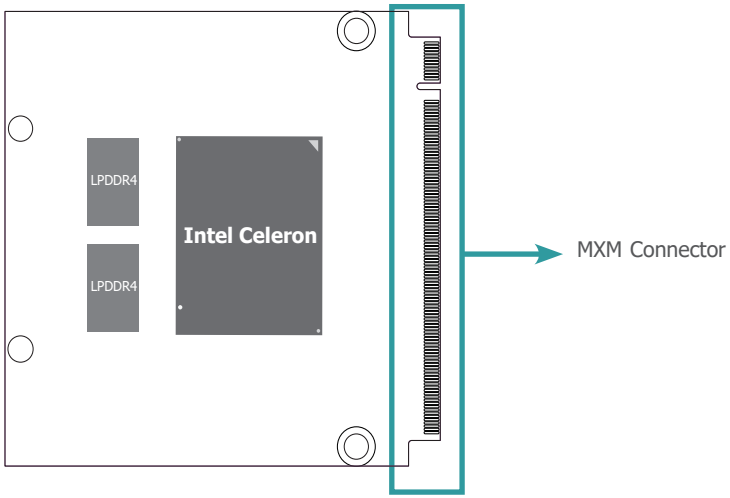
▶ System Memory

The system board is equipped with LPDDR4 memory chips onboard.



▶ MXM Connector

The MXM connector is used to interface with the carrier board. Insert EHL701 to the MXM connector on the carrier board. Refer to the following pages for the pin functions of this connector.



Important:

Boards, and other components. Perform installation procedures at an ESD workstation only.
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The table below is a comprehensive list of all signal pins supported on the 230-pin MXM connectors.

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
1	GND	GND	2	GND	GND
3	GBE_MDI3-	GBE_MDI3-	4	GBE_MDI2-	GBE_MDI2-
5	GBE_MDI3+	GBE_MDI3+	6	GBE_MDI2+	GBE_MDI2+
7	GBE_LINK100#	GBE_LED_100-	8	GBE_LED_1000-	GBE_LED_1000-
9	GBE_MDI1-	GBE_MDI1-	10	GBE_MDI0-	GBE_MDI0-
11	GBE_MDI1+	GBE_MDI1+	12	GBE_MDI0+	GBE_MDI0+
13	GBE_LINK#	GBE_LED_LINK-	14	GBE_ACT#	GBE_LED_ACT-
15	GBE_CTREF	NC	16	SUS_S5#	EC_PM_SLP_S4-
17	WAKE#	WAKE-	18	SUS_S3#	EC_PM_SLP_S3-
19	GPO0	GPIO0_C	20	PWRBTN#	CB_PWRBTN-
21	SLP_BTN# /GPII1	SLP_BTN-	22	LID_BTN# /GPII0	LID_BTN-
23	GND	GND	24	GND	GND
	KEY	KEY		KEY	KEY
25	GND	GND	26	PWGIN	CB_PWROK_C
27	BATLOW# /GPII2	GPIO2_C	28	RSTBTN#	SYS_RST-
29	SATA0_TX+	SATA_TX0P	30	SATA1_TX+	SATA_TX1P
31	SATA0_TX-	SATA_TX0N	32	SATA1_TX-	SATA_TX1N
33	SATA_ACT#	SATA_ACT-	34	GND	GND
35	SATA0_RX+	SATA_RX0P	36	SATA1_RX+	SATA_RX1P
37	SATA0_RX-	SATA_RX0N	38	SATA1_RX-	SATA_RX1N
39	GND	GND	40	GND	GND
41	BIOS_DISABLE# / BOOT_ALT#	BIOS_DIS0-	42	SDIO_CLK#	SDIO_CLK
43	SDIO_CD#	SDIO_CD-	44	RSVD	SDIO_LED

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
45	SDIO_CMD	SDIO_CMD	46	SDIO_WP	SDIO_WP
47	SDIO_PWR#	SDIO_PWR	48	SDIO_DAT1	SDIO_D1
49	SDIO_DAT0	SDIO_D0	50	SDIO_DAT3	SDIO_D3
51	SDIO_DAT2	SDIO_D2	52	RSVD	NC
53	RSVD	NC	54	RSVD	NC
55	RSVD	NC	56	USB_OTG_PEN	USB_OTG_PEN
57	GND	GND	58	GND	GND
59	HDA_SYNC / I2S_WS	HDA_SYNC_3V3	60	SMB_CLK / GP1_I2C_CLK	SMBCK_BTB
61	HDA_RST# / I2S_RST#	3V3_HDA_RST-	62	SMB_DAT / GP1_I2C_DAT	SMBDAT_BTB
63	HDA_BITCLK / I2S_CLK	HDA_BITCLK_3V3	64	SMB_ALERT#	SMB_ALERT-_EC_BTB
65	HDA_SDI / I2S_SDI	HDA_SDI0_3V3	66	GP0_I2C_CLK	I2C_SCL1
67	HDA_SDO / I2S_SDO	HDA_SDO_3V3	68	GP0_I2C_DAT	I2C_SDA1
69	THRM#	THRM-	70	WDTRIG#	WDTRIG#_C
71	THRMTRIP#	THERMTRIP-	72	WDOUT	WDOUT_C
73	GND	GND	74	GND	GND
75	USB_P7- / USB_SSTX0-	USB3_TXP0N (option USB_P7-)	76	USB_P6- / USB_SSRX0-	USB3_RXP0N (option USB_P6-)
77	USB_P7+ / USB_SSTX0+	USB3_TXP0P (option USB_P7+)	78	USB_P6+ / USB_SSRX0+	USB3_RXP0P (option USB_P6+)
79	USB_6_7_OC#	USB67_OC-	80	USB_4_5_OC#	USB45_OC-
81	USB_P5- / USB_SSTX2-	USB3_TXP2N (option USB_P5-)	82	USB_P4- / USB_SSRX2-	USB3_RXP2N (option USB_P4-)
83	USB_P5+ / USB_SSTX2+	USB3_TXP2P (option USB_P5+)	84	USB_P4+ / USB_SSRX2+	USB3_RXP2P (option USB_P4+)
85	USB_2_3_OC#	USB23_OC-	86	USB_0_1_OC#	USB01_OC-

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
87	USB_P3-	USB2_DN3	88	USB_P2-	USB2_DN2
89	USB_P3+	USB2_DP3	90	USB_P2+	USB2_DP2
91	USB_VBUS	USB_VBUS_SUS_C	92	USB_ID	USB_OTG_ID_3V3
93	USB_P1-	USB2_DN0	94	USB_P0-	USB2_DN1
95	USB_P1+	USB2_DP0	96	USB_P0+	USB2_DP1
97	GND	GND	98	GND	GND
99	eDP0_TX0+ / LVDS_A0+	LVDSA_0+_R (option eDP0_TX0+)	100	eDP1_TX0+ / LVDS_B0+	LVDS_B0+_R (option eDP1_TX0+)
101	eDP0_TX0- / LVDS_A0-	LVDSA_0-_R (option eDP0_TX0-)	102	eDP1_TX0- / LVDS_B0-	LVDS_B0-_R (option eDP1_TX0-)
103	eDP0_TX1+ / LVDS_A1+	LVDSA_1+_R (option eDP0_TX1+)	104	eDP1_TX1+ / LVDS_B1+	LVDS_B1+_R (option eDP1_TX1+)
105	eDP0_TX1- / LVDS_A1-	LVDSA_1-_R (option eDP0_TX1-)	106	eDP1_TX1- / LVDS_B1-	LVDS_B1-_R (option eDP1_TX1-)
107	eDP0_TX2+ / LVDS_A2+	LVDSA_2+_R (option eDP0_TX2+)	108	eDP1_TX2+ / LVDS_B2+	LVDS_B2+_R (option eDP1_TX2+)
109	eDP0_TX2- / LVDS_A2-	LVDSA_2-_R (option eDP0_TX2-)	110	eDP1_TX2- / LVDS_B2-	LVDS_B2-_R (option eDP1_TX2-)
111	LVDS_PPEN	LVDS_VDD_EN_R	112	LVDS_BLEN	LVDS_BKLT_EN_R
113	eDP0_TX3+ / LVDS_A3+	LVDSA_3+_R (option eDP0_TX3+)	114	eDP1_TX3+ / LVDS_B3+	LVDS_B3+_R (option eDP1_TX3+)
115	eDP0_TX3- / LVDS_A3-	LVDSA_3-_R (option eDP0_TX3-)	116	eDP1_TX3- / LVDS_B3-	LVDS_B3-_R (option eDP1_TX3-)
117	GND	GND	118	GND	GND
119	eDP0_AUX+ / LVDS_A_CLK+	LVDS_A_CK+ (option eDP0_AUX+)	120	eDP1_AUX+ / LVDS_B_CLK+	LVDS_B_CLK+_R (option eDP1_AUX+)
121	eDP0_AUX- / LVDS_A_CLK-	LVDS_A_CK- (option eDP0_AUX-)	122	eDP1_AUX- / LVDS_B_CLK-	LVDS_B_CLK-_R (option eDP1_AUX-)
123	LVDS_BLT_CTRL / GP_PWM_OUT0	LVDS_BKLT_CTRL_R	124	GP_1-Wire_Bus / HDMI_CEC	GP_1-Wire_Bus
125	GP2_I2C_DAT / LVDS_DID_DAT	LVDS_DDC_DATA_R (option eDP1_DDC_DAT)	126	eDP0_HPD# / LVDS_BLC_DAT	eDP_HPD#_C
127	GP2_I2C_CLK / LVDS_DID_CLK	LVDS_DDC_CLK_R (option eDP1_DDC_CLK)	128	eDP1_HPD# / LVDS_BLC_CLK	DDI1_HPD#_C
129	CAN0_TX	NC	130	CAN0_RX	NC

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
131	DP_LANE3+ / TMDS_CLK+	DDI0_3P	132	USB_SSTX1-	USB3_P1_TXN_C
133	DP_LANE3- / TMDS_CLK-	DDI0_3N	134	USB_SSTX1+	USB3_P1_TXP_C
135	GND	GND	136	GND	GND
137	DP_LANE1+ / TMDS_LANE1+	DDI0_1P	138	DP_AUX+	DPI0_AUX_C_P
139	DP_LANE1- / TMDS_LANE1-	DDI0_1N	140	DP_AUX-	DPI0_AUX_C_N
141	GND	GND	142	GND	GND
143	DP_LANE2+ / TMDS_LANE0+	DDI0_2P	144	USB_SSRX1-	USB3_P1_RXN
145	DP_LANE2- / TMDS_LANE0-	DDI0_2N	146	USB_SSRX1+	USB3_P1_RXP
147	GND	GND	148	GND	GND
149	DP_LANE0+ / TMDS_LANE2+	DDI0_0P	150	HDMI_CTRL_DAT	DDI0_DDC_SDA_C
151	DP_LANE0- / TMDS_LANE2-	DDI0_0N	152	HDMI_CTRL_CLK	DDI0_DDC_SCL_C
153	HDMI_HPD#	DDI0_HDMI_HPD	154	DP_HPD#	DDI0_DP_HPD
155	PCIE_CLK_REF+	PCIE_CLK_REF+	156	PCIE_WAKE#	PCIE_WAKE2-
157	PCIE_CLK_REF-	PCIE_CLK_REF-	158	PCIE_RST#	CB_PLTRST-_BUFF
159	GND	GND	160	GND	GND
161	PCIE3_TX+	PCIE_P3_TXP_C	162	PCIE3_RX+	PCIE_P3_RXP
163	PCIE3_TX-	PCIE_P3_TXN_C	164	PCIE3_RX-	PCIE_P3_RXN
165	GND	GND	166	GND	GND
167	PCIE2_TX+	PCIE_P2_TXP_C	168	PCIE2_RX+	PCIE_P2_RXP
169	PCIE2_TX-	PCIE_P2_TXN_C	170	PCIE2_RX-	PCIE_P2_RXN

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
171	UART0_TX	EC_SOUT1	172	UART0_RTS#	EC_RTS1#
173	PCIE1_TX+	PCIE_P1_TXP_C	174	PCIE1_RX+	PCIE_P1_RXP
175	PCIE1_TX-	PCIE_P1_TXN_C	176	PCIE1_RX-	PCIE_P1_RXN
177	UART0_RX	EC_SIN1	178	UART0_CTS#	EC_CTS1#
179	PCIE0_TX+	PCIE_P0_TXP_C	180	PCIE0_RX+	PCIE_P0_RXP
181	PCIE0_TX-	PCIE_P0_TXN_C	182	PCIE0_RX-	PCIE_P0_RXN
183	GND	GND	184	GND	GND
185	LPC_AD0 / GPIO0	LPC_AD0	186	LPC_AD1 / GPIO1	LPC_AD1
187	LPC_AD2 / GPIO2	LPC_AD2	188	LPC_AD3 / GPIO3	LPC_AD3
189	LPC_CLK / GPIO4	CLK1_25M_CB	190	LPC_FRAME# / GPIO5	LPC_FRAME-
191	SERIRQ / GPIO6	LPC_SERIRQ	192	LPC_LDRQ# / GPIO7	NC
193	VCC_RTC	V_3P0_BAT	194	SPKR / GP_PWM_OUT2	HDA_SPKR_3V3
195	FAN_TACHOIN / GP_ TIMER_IN	SYSFAN	196	FAN_PWMOUT / GP_ PWM_OUT1	PWMOUT
197	GND	GND	198	GND	GND
199	SPI_MOSI	SPI_MOSI_D0_3VSB	200	SPI_CS0#	SPI_CS0_CB

Pin	Q7 R2.1 Signal	EHL701 Signal	Pin	Q7 R2.1 Signal	EHL701 Signal
201	SPI_MISO	SPI_MISO_D1_3VSB	202	SPI_CS1#	NC
203	SPI_SCK	SPI_CLK_3VSB	204	MFG_NC4	NC
205	VCC_5V_SB	5VSB_P	206	VCC_5V_SB	VCC_5V_SB
207	MFG_NC0	NC	208	MFG_NC2	NC
209	MFG_NC1	NC	210	MFG_NC3	NC
211	NC	NC	212	NC	NC
213	NC	NC	214	NC	NC
215	NC	NC	216	NC	NC
217	NC	NC	218	NC	NC
219	VCC	CB_VIN	220	VCC	CB_VIN
221	VCC	CB_VIN	222	VCC	CB_VIN
223	VCC	CB_VIN	224	VCC	CB_VIN
225	VCC	CB_VIN	226	VCC	CB_VIN
227	VCC	CB_VIN	228	VCC	CB_VIN
229	VCC	CB_VIN	230	VCC	CB_VIN

▶ MXM Connector Signal Description

Pin Types
I Input Pin
O Output Pin
I/O Bi-directional input / output Pin
OD Open drain
PP Push Pull
NC Not Connected

PCI Express Interface Signals Descriptions						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
PCIE_RX0P	180		PCIE		**Device** - Connect AC Coupling cap 0.1uF	
PCIE_RX0N	182	I PCIE	PCIE		**Slot** - Connect to PCIE Conn pin	PCI Express channel 0, Receive Input differential pair.
PCIE_TX0P	179		PCIE	AC Coupling capacitor		
PCIE_TX0N	181	O PCIE	PCIE	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express channel 0, Transmit Output differential pair.
	174				**Device** - Connect AC Coupling cap 0.1uF	
PCIE_RX1P	176	I PCIE	PCIE		**Slot** - Connect to PCIE Conn pin	PCI Express channel 1, Receive Input differential pair.
PCIE_RX1N	173			AC Coupling capacitor		
PCIE_TX1P	175	O PCIE	PCIE	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express channel 1, Transmit Output differential pair.
PCIE_TX1N	168				**Device** - Connect AC Coupling cap 0.1uF	
PCIE_RX2P	170	I PCIE	PCIE		**Slot** - Connect to PCIE Conn pin	PCI Express channel 2, Receive Input differential pair.
PCIE_RX2N	167			AC Coupling capacitor		
PCIE_TX2P	169	O PCIE	PCIE	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express channel 2, Transmit Output differential pair.
	162				**Device** - Connect AC Coupling cap 0.1uF (This Port is BOM Option with On	
PCIETX2N	164	I PCIE	PCIE		board LAN)	PCI Express channel 3, Receive Input differential pair.(This Port is BOM Option with On board LAN)
PCIRX3P	161			AC Coupling capacitor	Connect to PCIE device or slot (This Port is BOM Option with On board	
PCIE_RX3N	163	O PCIE	PCIE	AC Coupling capacitor	LAN)	PCI Express channel 3, Transmit Output differential pair.(This Port is BOM Option with On board LAN)
PCIE_T3P	155					
PCIE_TX3N PC	157	O PCIE	PCIE		Connect to PCIE device, PCIe CLK Buffer or slot	PCI Express Reference Clock for Lanes 0 to 3.
PCIE_WAKE	156	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend		PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.
PCIERST#_BTB	158	O CMOS	3.3V/3.3V			Reset Signal for external devices.

UART Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
SOUT1	171	O CMOS	3.3V/3.3V		Connect to SIO	Serial Data Transmitter
SIN1	177	I CMOS	3.3V/3.3V		Connect to SIO	Serial Data Reciever
CTS1#	178	I CMOS	3.3V/3.3V		Connect to SIO	Handshake signal, ready to send data
RTS1#	172	O CMOS	3.3V/3.3V		Connect to SIO	Handshake signal, ready to receive data

Gigabit Ethernet Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
GBE_MDI0+	12				Connect to Magnetics Module MDI0+/-	
GBE_MDI0-	10	I/O GB_LAN	GB_LAN			Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes.This signal pair is used for all modes.
GBE_MDI1+	11				Connect to Magnetics Module MDI0+/-	
GBE_MDI1-	9	I/O GB_LAN	GB_LAN			Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes.This signal pair is used for all modes.
GBE_MDI2+	6				Connect to Magnetics Module MDI0+/-	
GBE_MDI2-	4	I/O GB_LAN	GB_LAN			Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes.This signal pair is used for all modes.
GBE_MDI3+	5				Connect to Magnetics Module MDI0+/-	
GBE_MDI3-	3	I/O GB_LAN	GB_LAN			Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.This signal pair is used for all modes.
NC	15	REF		NC		Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less
GBE_LED_LINK-	13	O CMOS 3.3V PP	3.3V/3.3V			Ethernet controller 0 link indicator, active low.
GBE_LED_100-	7	O CMOS 3.3V PP	3.3V/3.3V			Ethernet controller 0 100Mbit/sec link indicator, active low.
GBE_LED_1000-	8	O CMOS 3.3V PP	3.3V/3.3V			Ethernet controller 0 1000Mbit/sec link indicator, active low.
GBE_LED_ACT-	14	O CMOS 3.3V PP	3.3V/3.3V			Ethernet controller 0 activity indicator, active low.

USB Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
USB3_P1_RXP	146	I USB			Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	USB Superspeed receive signal differential pair
USB3_P1_RXN	144	I USB	USB		to GND to USB connector	USB Superspeed receive signal differential pair
USB3_P1_TXP_C	134	O USB		AC Coupling capacitor	Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	USB Superspeed receive signal differential pair
USB3_P1_TXN_C	132	O USB	USB	AC Coupling capacitor	to GND to USB connector	USB Superspeed receive signal differential pair
USB2_DP1	96				Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	
USB2_D1N	94	I/O USB	USB		to GND to USB connector	Universal Serial Bus Port 0 differential pair
USB2_DP0	95				Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	
USB2_DN0	93	I/O USB	USB		to GND to USB connector	Universal Serial Bus Port 1 differential pair.This port may be optionally used as USB client port.
USB2_DP2	90				Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	
USB2_DN2	88	I/O USB	USB		to GND to USB connector	Universal Serial Bus Port 2 differential pair.
USB2_DP3	89				Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	
USB2_DN3	87	I/O USB	USB		to GND to USB connector	Universal Serial Bus Port 3 differential pair.
USB3_RXP2P (option USB_P4+)	84	I/O USB			Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	Universal Serial Bus Port 4 differential pair.
USB3_RXP2N (option USB_P4-)	82	I USB	USB		to GND to USB connector	Multiplexed with receive signal differential pairs for the Superspeed USB data path.
USB3_TXP2P (option USB_P5+)	83	I/O USB		AC Coupling capacitor	Connect 90 Ω @100MHz Common Choke in series and ESD suppressors	Multiplexed with transmit signal differential pairs for the Superspeed USB data path.
USB3_TXP2N (option USB_P5-)	81	O USB	USB	AC Coupling capacitor	to GND to USB connector	
USB3_RXP0P (option USB_P6+)	78					Universal Serial Bus Port 6 differential pair.
USB3_RXP0N (option USB_P6-)	76	I/O USB I USB	USB			Multiplexed with receive signal differential pairs for the Superspeed USB data path
USB3_TXP0P (option USB_P7+)	77			AC Coupling capacitor		Universal Serial Bus Port 7 differential pair.
USB3_TXP0N (option USB_P7-)	75	I/O USB O USB	USB	AC Coupling capacitor	Connect Common Choke in series and ESD suppressors to GND to USB connector(This Port is BOM Option with USB_P6 / USB_P7)	Multiplexed with transmit signal differential pairs for the Superspeed USB data path
USB01_OC-	86	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	Connect to Overcurrent of USB Power Switch	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1
USB23_OC-	85	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	Connect to Overcurrent of USB Power Switch	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3
USB45_OC	80	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	Connect to Overcurrent of USB Power Switch	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5
USB67_OC-	79	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend	Connect to Overcurrent of USB Power Switch	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7
USB_OTG_ID_3V3	92	I CMOS	3.3V Suspend/3.3V			USB ID pin.Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.
USB_VBUS_SUS_C	91	I CMOS	CMOS 5.0V			USB VBUS pin, 5V tolerant VBUS resistance has to be placed on the module VBUS capacitance has to be placed on the carrier board
USB_OTG_PEN	56	O CMOS	CMOS 3.3V			USB Power enable pin for USB Port 1 Enables the Power for the USB-OTG port on the carrier board.

SDIO Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
SDIO_CD-	43	I/O CMOS	3.3V/3.3V		Connect to SD Card	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.
SDIO_CLK	42	O CMOS	3.3V/3.3V		Connect to SD Card	MHz
SDIO_CMD	45	I/O OD/PP CMOS	3.3V/3.3V		Connect to SD Card	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.
SDIO_WP	46	I/O CMOS	3.3V/3.3V		Connect to SD Card	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards
SDIO_PWR	47	O CMOS	3.3V/3.3V		Connect to SD Card	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.
SDIO_D1	48	I/O PP CMOS	3.3V/3.3V		Connect to SD Card	SDIO Data lines. These signals operate in push-pull mode
SDIO_D0	49	I/O PP CMOS	3.3V/3.3V		Connect to SD Card	SDIO Data lines. These signals operate in push-pull mode
SDIO_D3	50	I/O PP CMOS	3.3V/3.3V		Connect to SD Card	SDIO Data lines. These signals operate in push-pull mode
SDIO_D2	51	I/O PP CMOS	3.3V/3.3V		Connect to SD Card	SDIO Data lines. These signals operate in push-pull mode

High Definition Audio Signals/AC'97						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
3V3_HDA_RST-	61	O CMOS	3.3V/3.3V		Connect to CODEC	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset.
HDA_SYNC_3V3	59	O CMOS	3.3V/3.3V		Connect to CODEC	Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.
HDA_BITCLK_3V3	63	O CMOS	3.3V/3.3V		Connect to CODEC	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.
HDA_SDO_3V3	67	O CMOS	3.3V/3.3V		Connect to CODEC	HD Audio/AC'97 Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec
HDA_SDI0_3V3	65	I CMOS	3.3V/3.3V		Connect to CODEC	HD Audio/AC'97 Serial Data input to Codec. Multiplexed with I2S Serial Data Input from Codec.

EDP Flat Panel Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
LVDS_VDD_EN_R	111	O CMOS	3.3V/3.3V		Connect to enable control of LVDS panel power circuit	Controls panel power enable.
LVDS_BKLT_EN_R	112	O CMOS	3.3V/3.3V		Connect to enable control of LVDS panel backlight power circuit.	Controls panel Backlight enable.
LVDS_BKLT_CTRL_R	123	O CMOS	3.3V/3.3V		Connect to brightness control of LVDS panel backlight power circuit.	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output
LVDSA_0+_R (option eDP0_TX0+)	99			eDP AC Coupling capacitor		
LVDSA_0-_R (option eDP0_TX0-)	101	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS primary channel differential pair 0. Display Port primary channel differential pair 0.
LVDSA_1+_R (option eDP0_TX1+)	103			eDP AC Coupling capacitor		
LVDSA_1-_R (option eDP0_TX1-)	105	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS primary channel differential pair 1. Display Port primary channel differential pair 1.
LVDSA_2+_R (option eDP0_TX2+)	107			eDP AC Coupling capacitor		
LVDSA_2-_R (option eDP0_TX2-)	109	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS primary channel differential pair 2. Display Port primary channel differential pair 2.
LVDSA_3+_R (option eDP0_TX3+)	113			eDP AC Coupling capacitor		
LVDSA_3-_R (option eDP0_TX3-)	115	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS primary channel differential pair 3. Display Port primary channel differential pair 3
LVDS_A_CK+ (option eDP0_AUX+)	119			eDP AC Coupling capacitor		
LVDS_A_CK- (option eDP0_AUX-)	121	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS primary channel differential pair clock lines. Display Port primary auxiliary channel.
LVDS_B0+_R (option eDP1_TX0+)	100			eDP AC Coupling capacitor		
LVDS_B0-_R (option eDP1_TX0-)	102	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS secondary channel differential pair 0. Display Port secondary channel differential pair 0.
LVDS_B1+_R (option eDP1_TX1+)	104			eDP AC Coupling capacitor		
LVDS_B1-_R (option eDP1_TX1-)	106	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	LVDS secondary channel differential pair 1. Display Port secondary channel differential pair 1.
LVDS_B2+_R (option eDP1_TX2+)	108			eDP AC Coupling capacitor		LVDS secondary channel differential pair 2.
LVDS_B2-_R (option eDP1_TX2-)	110	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	Display Port secondary channel differential pair 2
LVDS_B3+_R (option eDP1_TX3+)	114			eDP AC Coupling capacitor		LVDS secondary channel differential pair 3.
LVDS_BKLT_EN_R	112	O LVDS	LVDS	eDP AC Coupling capacitor	Connect to LVDS connector	Display Port secondary channel differential pair 3.
LVDS_B_CLK+_R (option eDP1_AUX+)	120					
LVDS_B_CLK-_R (option eDP1_AUX)	122	O LVDS	LVDS		Connect to LVDS connector	LVDS secondary channel differential pair clock lines. Display Port secondary auxiliary channel.
LVDS_DDC_CLK_R (option eDP1_DDC_CLK)	127	I/O OD CMOS	3.3V/3.3V	PU 2.2K to 3.3V	Connect to DDC clock of LVDS panel	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus clock line.
LVDS_DDC_DATA_R (option eDP1_DDC_DAT	125	I/O OD CMOS	3.3V/3.3V	PU 2.2K to 3.3V	Connect to DDC clock of LVDS panel	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be as General Purpose I²C bus data line.
DDI1_HPD#_C	128	I/O OD CMOS	3.3V/3.3V	NC		Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an embedded DisplayPort secondary Hotplug detection.
eDP_HPD#_C	126	I/O OD CMOS	3.3V/3.3V	NC		detection.

DisplayPort Interface Signal						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
DDI0_3N	133					
DDI0_3P	131	O PCIE	DP	AC Coupling capacitor		DisplayPort differential pair lines lane 3
DDI0_2N	145					
DDI0_2P	143	O PCIE	DP	AC Coupling capacitor		DisplayPort differential pair lines lane 2
DDI0_1N	139					
DDI0_1P	137	O PCIE	DP	AC Coupling capacitor		DisplayPort differential pair lines lane 1
DDI0_0N	151					
DDI0_0P	149	O PCIE	DP	AC Coupling capacitor		DisplayPort differential pair lines lane 0
DPI0_AUX_C_N	140				Connect AC Coupling Capacitors 0.1uF to Device, PU 100K to 3.3V	
DPI0_AUX_C_P	138	I/O PCIE	DP	AC Coupling capacitor	Connect AC Coupling Capacitors 0.1uF to Device, PD 100K to GND	Auxiliary channel used for link management and device control. Differential pair lines.
DDI0_DP_HPD	154	I CMOS	3.3V/3.3V	PU 10K to 3.3V		Hot plug detection signal that serves as an interrupt request

HDMI Interface Signal						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
DDI0_3N	133				Connect AC Coupling Capacitors 0.1uF to Device	
DDI0_3P	131	O TMDS	TMDS	AC Coupling capacitor	Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair clock lines.
DDI0_2N	145				Connect AC Coupling Capacitors 0.1uF to Device	
DDI0_2P	143	O TMDS	TMDS	AC Coupling capacitor	Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 0
DDI0_1N	139				Connect AC Coupling Capacitors 0.1uF to Device	
DDI0_1P	137	O TMDS	TMDS	AC Coupling capacitor	Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 1
DDI0_0N	151				Connect AC Coupling Capacitors 0.1uF to Device	
DDI0_0P	149	O TMDS	TMDS	AC Coupling capacitor	Connect AC Coupling Capacitors 0.1uF to Device	TMDS differential pair lines lane 2
DDI0_DDC_SCL_C	152	I/O OD CMOS	3.3V/3,3V	PU 2.2K to 3.3V		DDC based control signal (clock) for HDMI device. Note: Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.
DDI0_DDC_SDA_C	150	I/O OD CMOS	3.3V/3,3V	PU 2.2K to 3.3V		DDC based control signal (data) for HDMI device. Note: Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI
DDI0_HDMI_HPD	153	I CMOS	3.3V/3.3V	PU 10K to 3.3V		Hot plug detection signal that serves as an interrupt request.

LPC Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
LPC_AD[0..3]	185-188	I/O CMOS	3.3V/3.3V		Connect to LPC device	Multiplexed Command, Address and Data. General purpose input/output [0..3]
LPC_FRAME-	190	I/O CMOS	3.3V/3.3V		Connect to LPC device	LPC frame indicates the start of a new cycle or the termination of a broken cycle. General purpose input/output 5.
NC	192	I/O CMOS	3.3V/3.3V	NC		LPC DMA request. General purpose input/output 7.
CLK1_25M_CB	189	I/O CMOS	3.3V/3.3V		Connect to LPC device	LPC clock. General purpose input/output 4.
LPC_SERIRQ	191	I/O CMOS	3.3V/3.3V		Connect to LPC device	Serialized Interrupt. General purpose input/output 6.

SPI Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
SPI_MOSI_D0_3VSB	199	O CMOS	3.3V/3.3V		Connect a series resistor to Carrier Board SPI Device SI pin	Master serial output/Slave serial input signal. SPI serial output data from Qseven module to the SPI device.
SPI_MISO_D1_3VSB	201	I CMOS	3.3V/3.3V		Connect a series resistor to Carrier Board SPI Device SO pin	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven module.
SPI_CLK_3VSB	203	O CMOS	3.3V/3.3V		Connect a series resistor to Carrier Board SPI Device SCK pin	SPI clock output.
SPI_CS0_CB	200	O CMOS	3.3V/3.3V		Connect a series resistor to Carrier Board SPI Device CS# pin	SPI chip select 0 output.
NC	202	O CMOS	3.3V/3.3V	NC		SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.

CAN Bus Interface Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
NC	129	O CMOS	3.3V/3.3V	NC		High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.
NC	130	I CMOS	3.3V/3.3V	NC		Power Button: Low active power button input. This signal is triggered on the falling edge.

Power Management Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
SYS_RST-	28	I CMOS	3.3V/3.3V	PU 10K to 3.3V Suspend		Reset button input. This input may be driven active low by an external circuitry to reset the Qseven module.
GPIO2_C	27	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend		Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.
WAKE-	17	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend		External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.
EC_PM_SLP_S3-	18	O CMOS	3.3V Suspend/3.3V			S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.
EC_PM_SLP_S4-	16	O CMOS	3.3V Suspend/3.3V			S5 State: This signal indicates S4 or S5 (Soft Off) state.
SLP_BTN-	21	I CMOS	3.3V Suspend/3.3V			Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.
LID_BTN-	22	I CMOS	3.3V Suspend/3.3V			LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.

Miscellaneous Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
WDTRIG#_C	70	I CMOS	3.3V/3.3V	PU 10K to 3.3V Suspend		Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse
WDOUT_C	72	O CMOS	3.3V/3.3V	PU 10K to 3.3V Suspend		Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.
I2C_SCL1	66	I/O OD CMOS	3.3V/3.3V	PU 2.2K to 3.3V		General Purpose I²C bus #0 clock line.
I2C_SDA1	68	I/O OD CMOS	3.3V/3.3V	PU 2.2K to 3.3V		General Purpose I²C bus #0 data line
SMBCK_BTB	60	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend		Clock line of System Management Bus. Multiplexed with General Purpose I²C bus #1 clock line.
SMB_ALERT-_EC_BTB	62	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend		Data line of System Management Bus. Multiplexed with General Purpose I²C bus #1 data line.
SMB_ALERT-_EC_BTB	64	I/O OD CMOS	3.3V Suspend/3.3V	PU 10K to 3.3V Suspend		System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.
HDA_SPKR_3V3	194	O CMOS	3.3V/3.3V			Primary functionality is output for audio enunciator, the"speaker" in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.
BIOS_DIS0-	41	I CMOS	3.3V/3.3V	PU 10K to 3.3V Suspend		Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.
RSVD	52,53,53,55	NC		NC		Do not connect
GP_1-Wire_Bus	124	I/O CMOS	3.3V/3.3V			General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI
GPIO0_C	19	O CMOS	CMOS 3.3V			General Purpose Output 0

Manufacturing Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
NC	207	N.A	N.A	NC		This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.
NC	209	N.A	N.A	NC		This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.
NC	208	N.A	N.A	NC		This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal
NC	210	N.A	N.A	NC		This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.
NC	204	N.A	N.A	NC		This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.

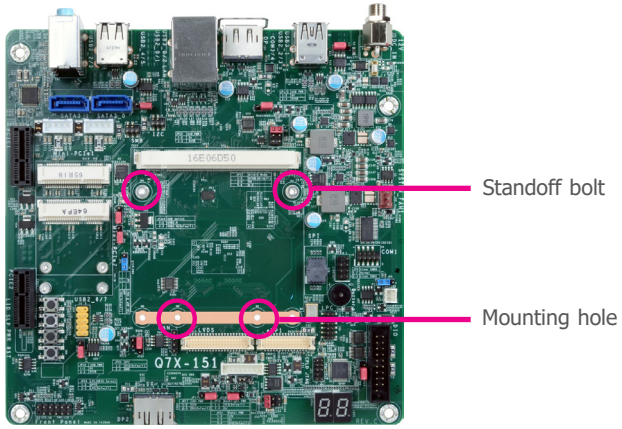
Thermal Management Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
THRM-	69	I CMOS	3.3V/3.3V	PU 10K to 3.3V		Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.
THERMTRIP-	71	O CMOS	3.3V/3.3V	PU 10K to 3.3V		Off).

Fan Control Implementation						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
PWMOUT	196	O OC CMOS	3.3V/3.3V			Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.
SYSFAN	195	I CMOS	3.3V/3.3V			Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.

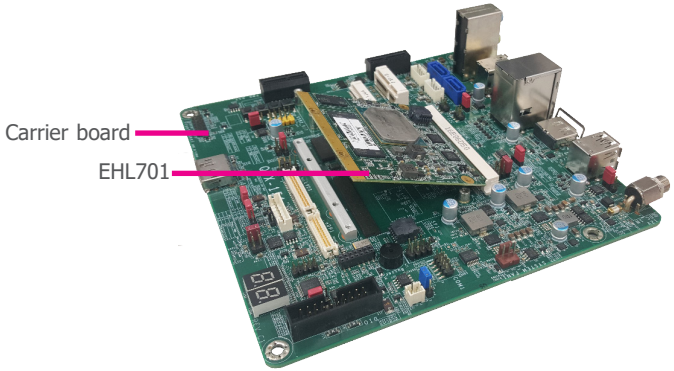
Miscellaneous Signals						
Signal	**Pin#**	**Pin Type**	**Pwr Rail /Tolerance**	**EHL701**	**Carrier Board**	**Description**
CB_VIN	219-230	Power				Power Supply +5VDC ±5%
VCC_5V_SB	205-206	Power				Standby Power Supply +5VDC ±5%
V_3P0_BAT	193	Power				3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).
GND	1-2, 23-25, 34, 39-40, 57-58, 73-74, 97-98, 117-118, 135-136, 141-142, 147-148, 159-160, 165-166, 183-184, 197-198	Power Ground			Power Ground.	
NC	211-218	NC				NC

▶ Installing EHL701 onto a Carrier Board

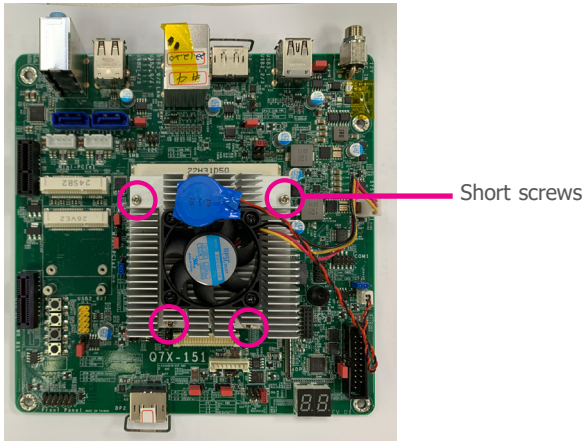
1. The photo below shows the locations of the mounting holes and the bolts already fixed in place.



2. Grasping EHL701 by its edges, insert it into the carrier board, and you will hear a distinctive ”click” indicating EHL701 is correctly locked into position.



3. Press down EHL701 and put on the heat sink on top of it with its mounting holes and bolts aligned on the carrier board. Use the mounting screws to fix EHL701 and heat sink in place.



Important:
The carrier board used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install EHL701 onto the carrier board of your choice.

Chapter 3 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<Esc>	Exits to the BIOS setup utility
+ (plus key)	Scrolls forward through the values or options of the hightlighted field.
- (minus key)	Scolls backward through the values or options of the hightlighted field.
<F1>	Displays general help
<F2>	Displays previous values
<F9>	Optimized defaults
<F10>	Saves and reset the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu

Scroll Bar

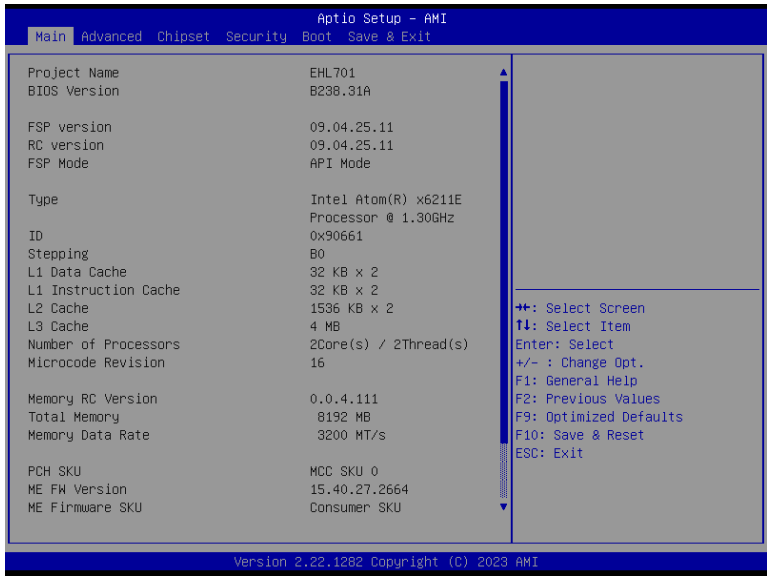
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Press "Tab" to switch to the next field and press "-" or "+" to modify the value.

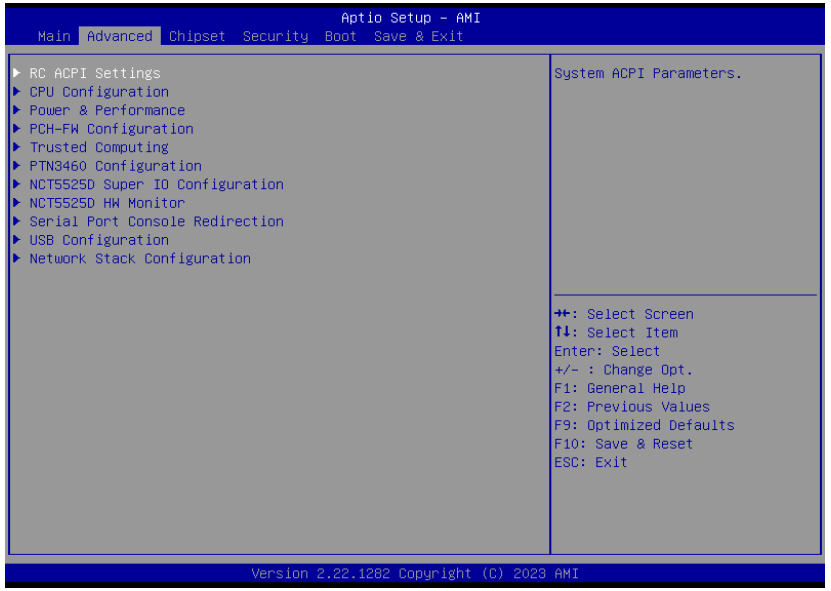
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

▶ Advanced

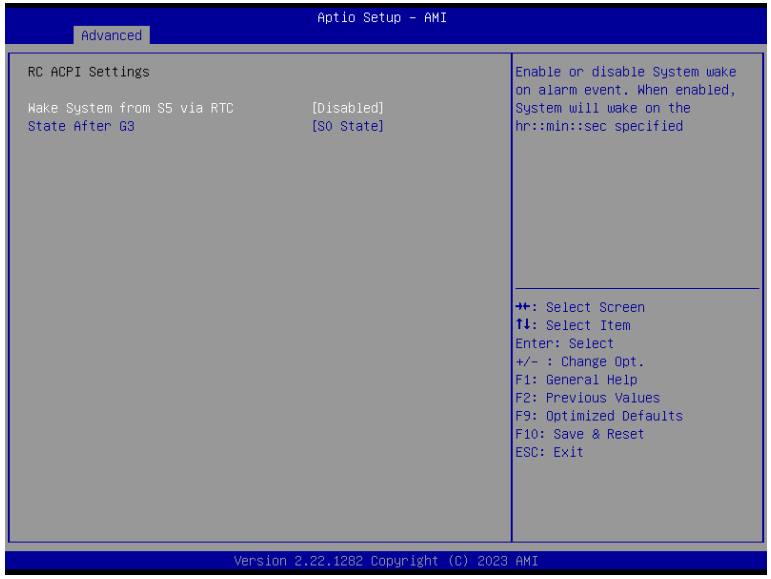
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

RC ACPI Configuration



Wake system from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

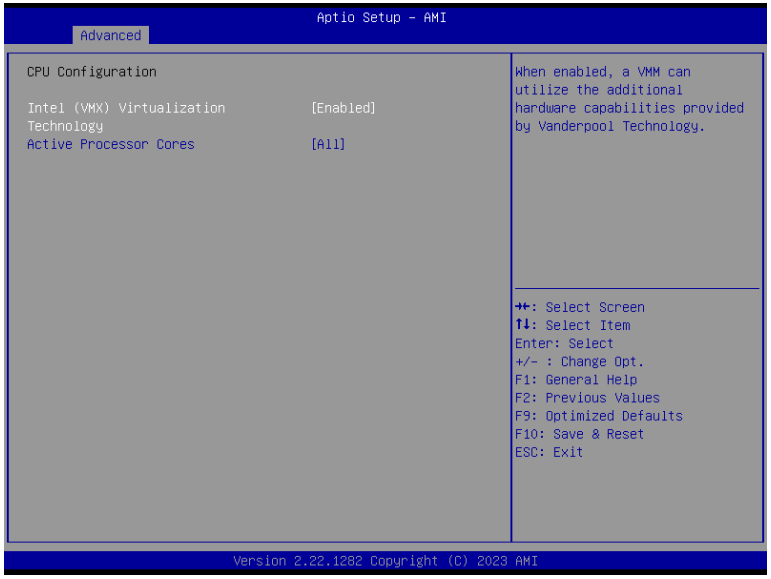
State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

- **S0 State** The system automatically powers on after power failure.
- **S5 State** The system enter soft-off state after power failure. Power-on signal input is required to power up the system.
- **Last State** The system returns to the last state right before power failure.

▶ Advanced

CPU Configuration



Intel (VMX) Virtualization Technology

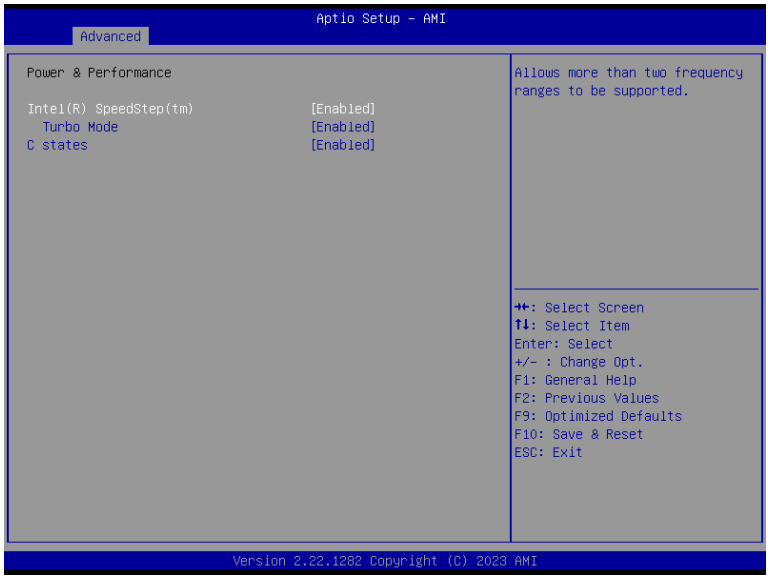
When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

Select number of cores to enable in each processor package.

▶ Advanced

Power & Performance



Intel(R) SpeedStep(tm)

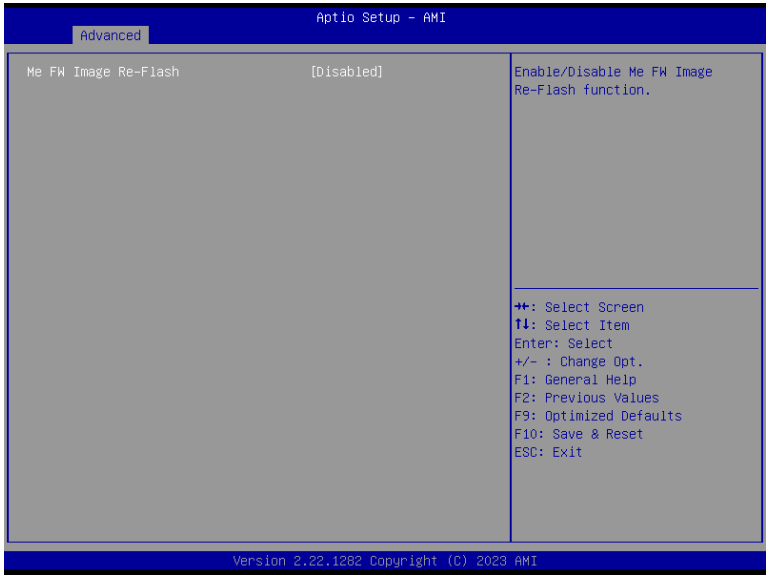
This field is used to enable or disable the Intel SpeedStep® Technology, which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

C states

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's idle and nothing is executing.

▶ Advanced

PCH-FW Configuration

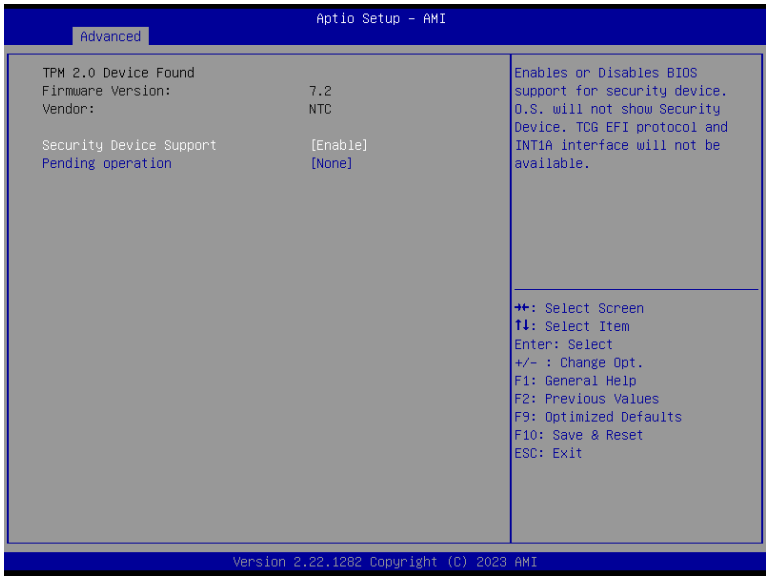


ME FW Image Re-Flash

Enable / Disable Me FW Image Re-Flash function.

▶ Advanced

Trusted Computing



Security Device Support

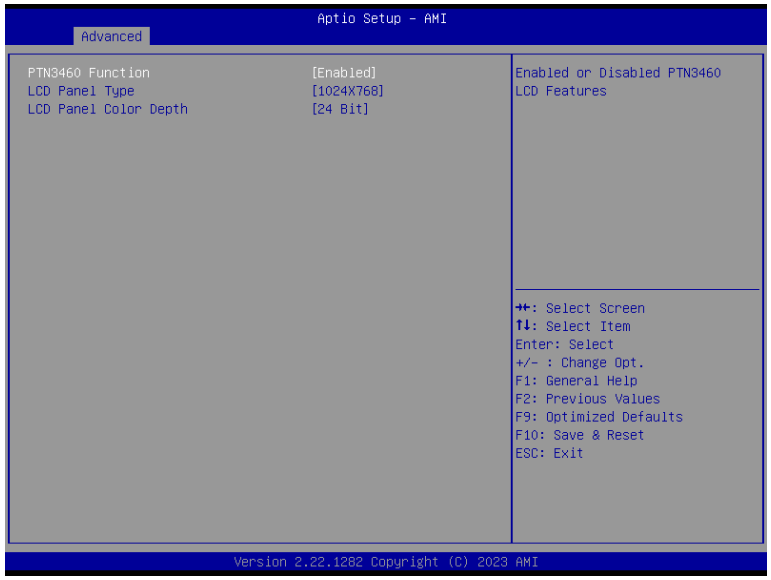
This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

▶ Advanced

PTN3460 Configuration



PTN3460 Function

Enabled or Disabled PTN3460 LCD Features.

LCD Panel Type

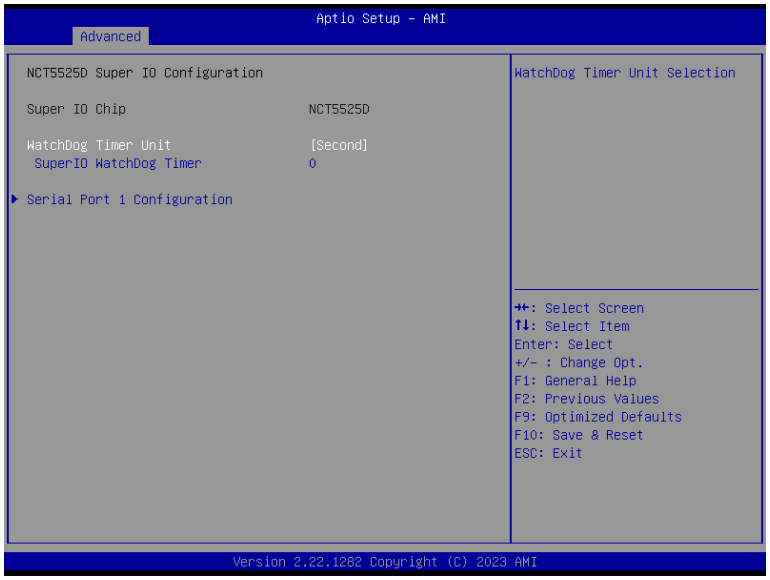
Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1024X600, 1280X800.

LCD Panel Color Depth

Select the color depth of the LCD Panel — 18 Bit, 24 Bit.

▶ Advanced

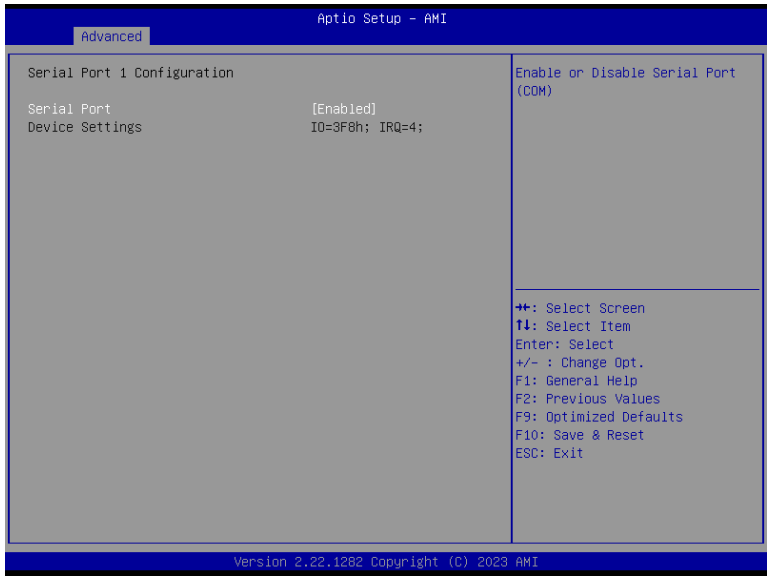
NCT5525D Super IO Configuration



Serial Port Configuration
Set Parameters of Serial Ports. See next page.

▶ Advanced

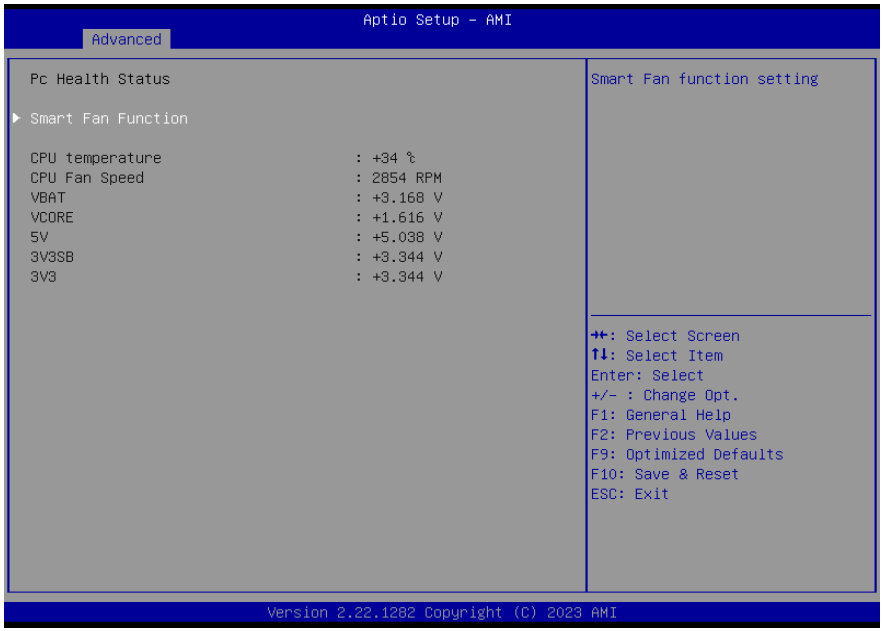
NCT5525D Super IO Configuration ▶ Serial Port 1 Configuration



Serial Port
Enable or disable serial port.

▶ Advanced

NCT5525D HW Monitor



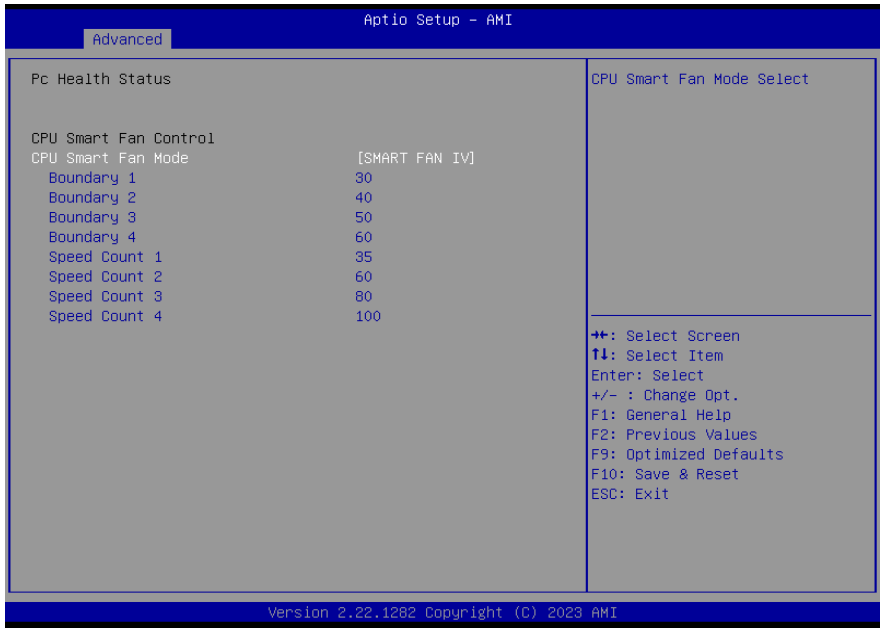
This section displays the system's health information, i.e. voltage readings, CPU and system temperatures, and fan speed readings

Smart Fan Function

Smart Fan Function Setting.

▶ Advanced

NCT5525D HW Monitor ▶ Smart FAN Function



▼ CPU Smart Fan Mode = [Smart Fan]

Boundary 1 to Boundary 4

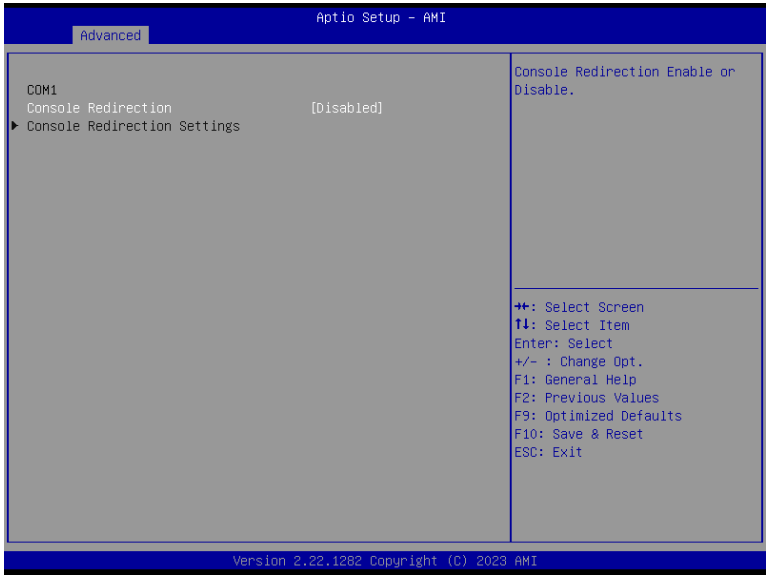
Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127℃. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

Fan Speed Count 1 to Fan Speed Count 4

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

▶ Advanced

Serial Port Console Redirection

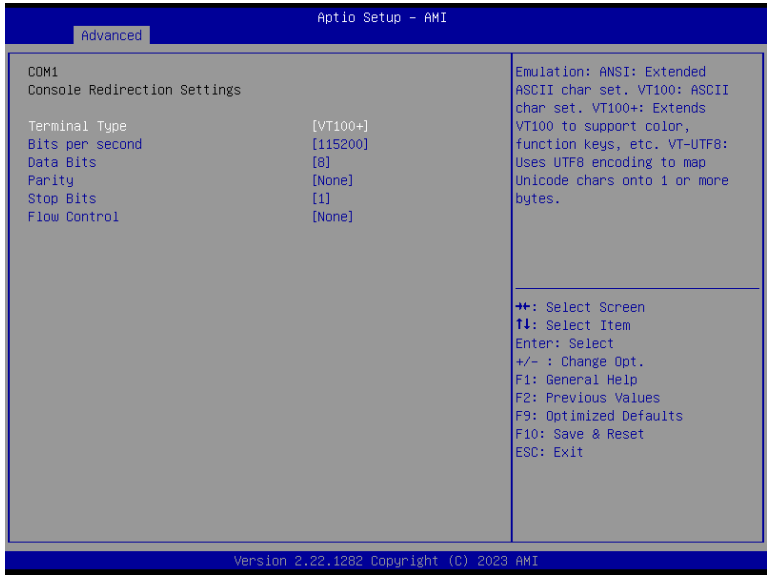


Console Redirection
Console Redirection Enable or Disable.

Console Redirection Settings
See following pages.

▶ Advanced

Serial Port Console Redirection ▶ Console Redirection Settings



Configure the serial settings of the current COM port.

Terminal Type
Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second
Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits
Select data bits: 7 bits or 8 bits.

Parity
Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits
Select stop bits: 1 bit or 2 bits.

Flow Control
Select flow control type: None or Hardware RTS/CTS. Flow Control is for RS485 mode.

▶ Advanced

USB Configuration

XHCI Hand-off

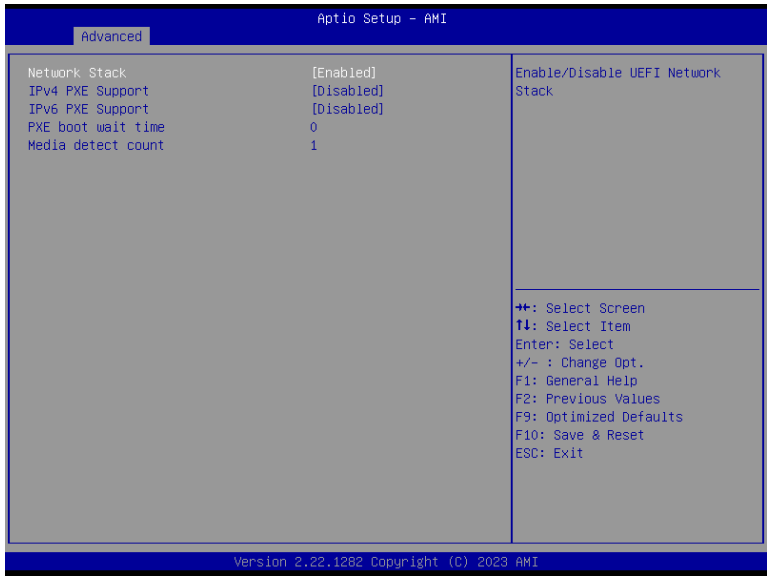
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

▶ Advanced

Network Stack Configuration



Network Stack

Enable or disable (Default) UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

PXE boot wait time

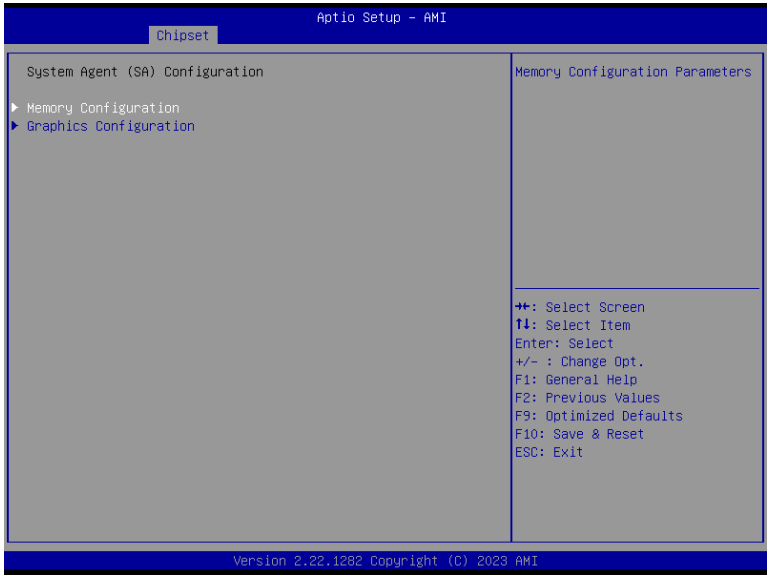
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

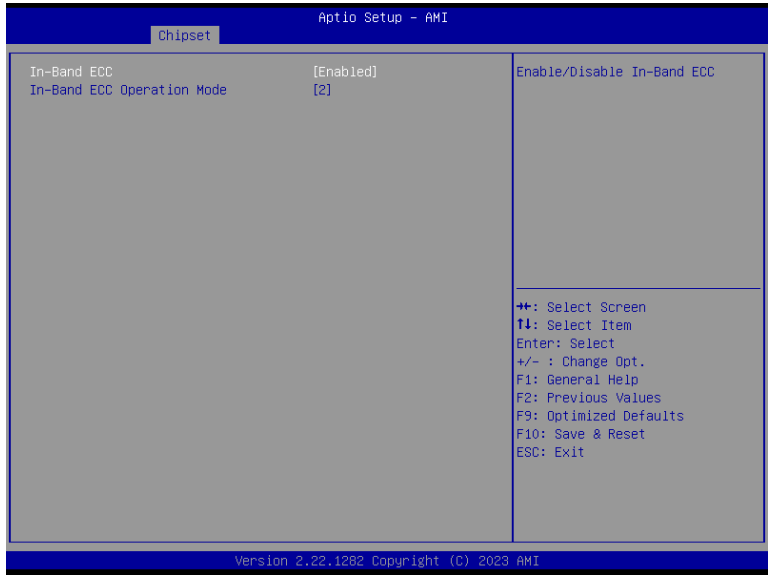
Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Chipset

System Agent (SA) Configuration



System Agent (SA) Configuration ▶ Memory Configuration



In-Band ECC

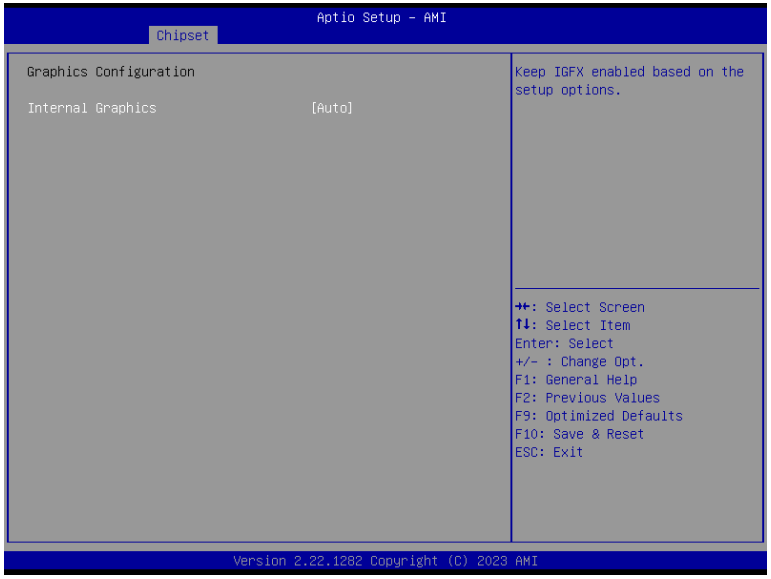
Enable/Disable (Default) In-Band ECC

In-Band ECC Operation Mode

0: Functional Mode protects requests based on the address range,
1: Makes all requests non protected and ignore range checks,
2: Makes all requests protected and ignore range checks

.

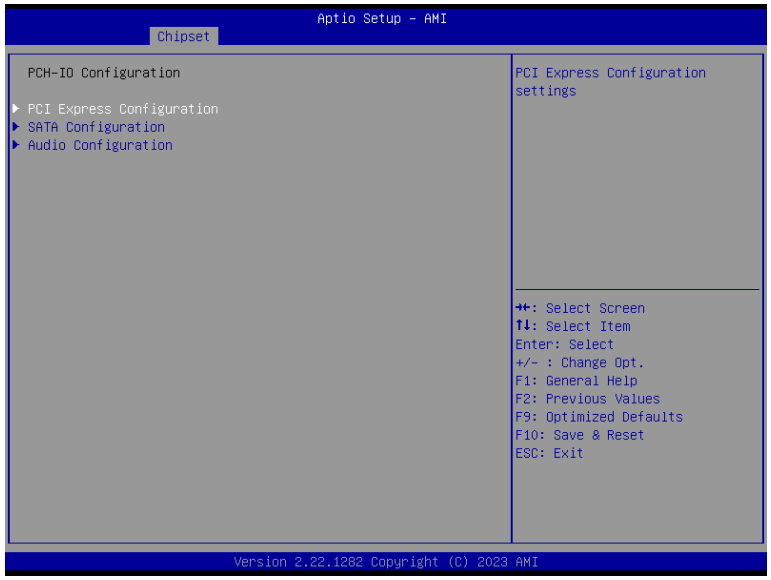
System Agent (SA) Configuration ▶ Graphics Configuration



Internal Graphics

Keep IGFX "Enabled" or "Disabled" based on the setup options, or select "Auto" for auto-detection.

PCH-IO Configuration



PCI Express Configuration

PCI Express Configuration Settings

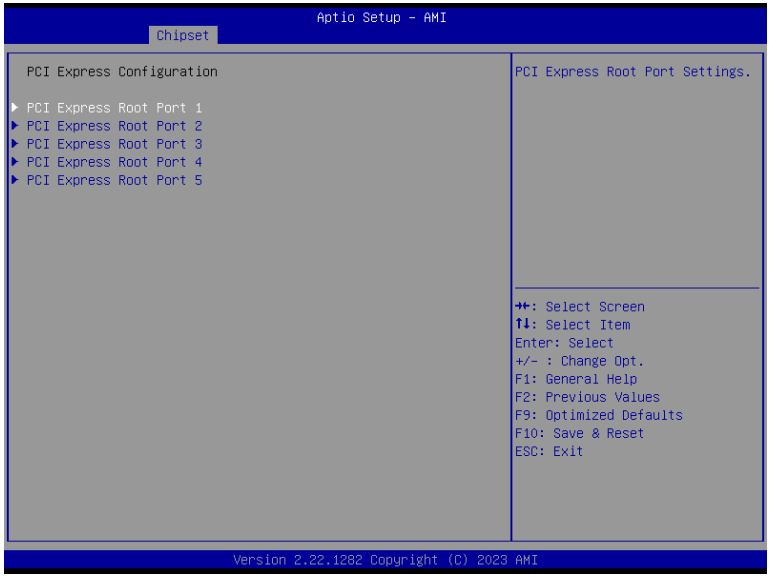
SATA Configuration

SATA Device Otpions Settings

HD Audio Configuration

HD Audio Subsystem Configuration Settings

PCH-IO Configuration ▶ PCI Express Configuration



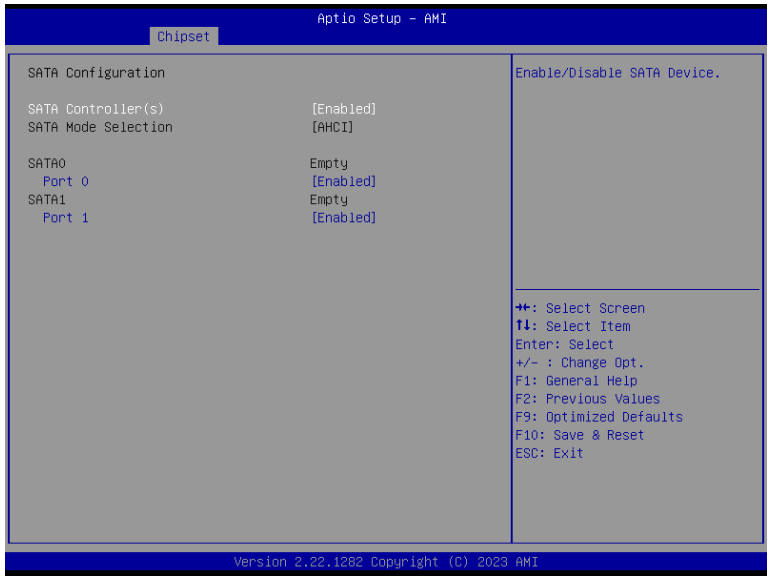
Select one of the PCI Express channels and press enter to configure the following settings.

PCIe Express Root Port 1,2,3,4

Control the PCI Express Root Port.

▶ Chipset

PCH-IO Configuration ▶ SATA Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

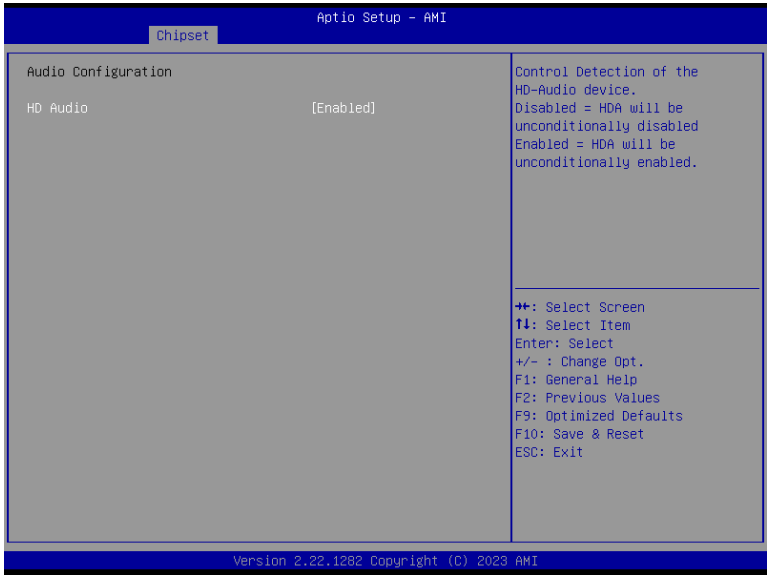
- **AHCI** This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

Ports

Enable or disable the Serial ATA ports.

▶ Chipset

PCH-IO Configuration ▶ Audio Configuration

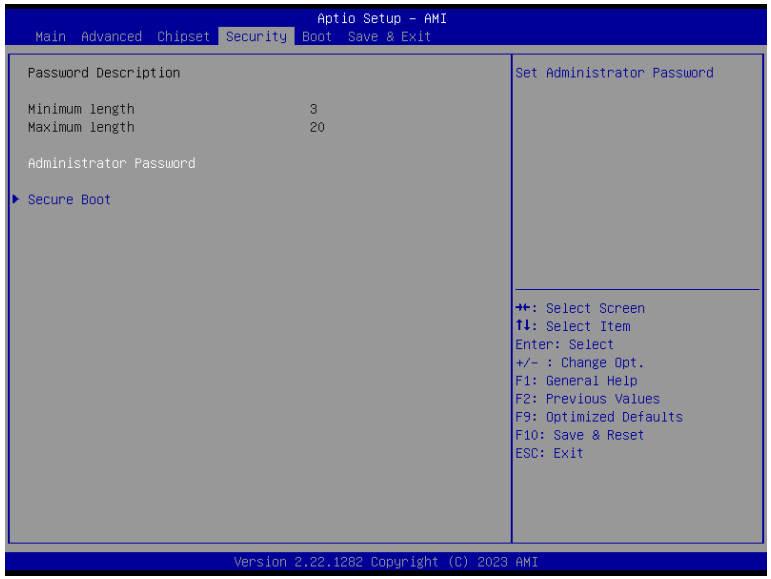


HD Audio

Control the detection of the HD Audio device.

- **Disabled** HDA will be unconditionally disabled.
- **Enabled** HDA will be unconditionally enabled.

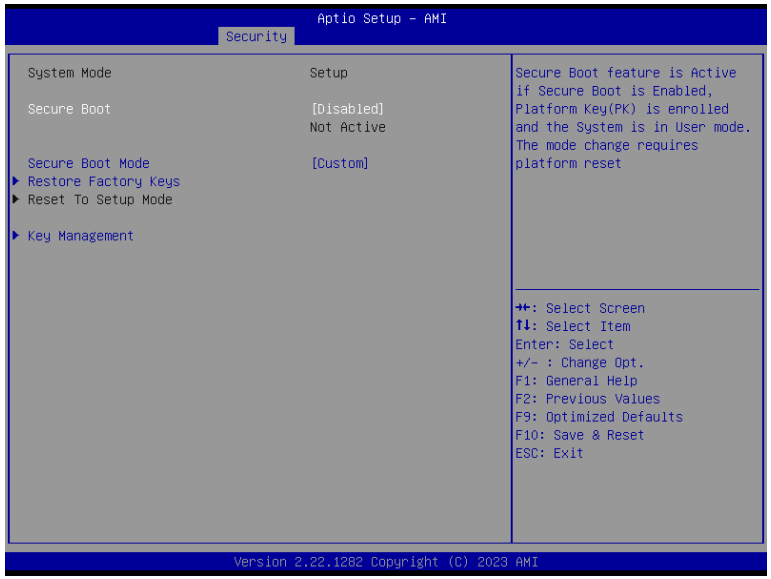
▶ Security



Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

Secure Boot



Secure Boot

Secure Boot feature is Active if secure Boot is Enabled, Platform Key (PK) is enrolled and the system is in user mode. The mode change requires platform reset.

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

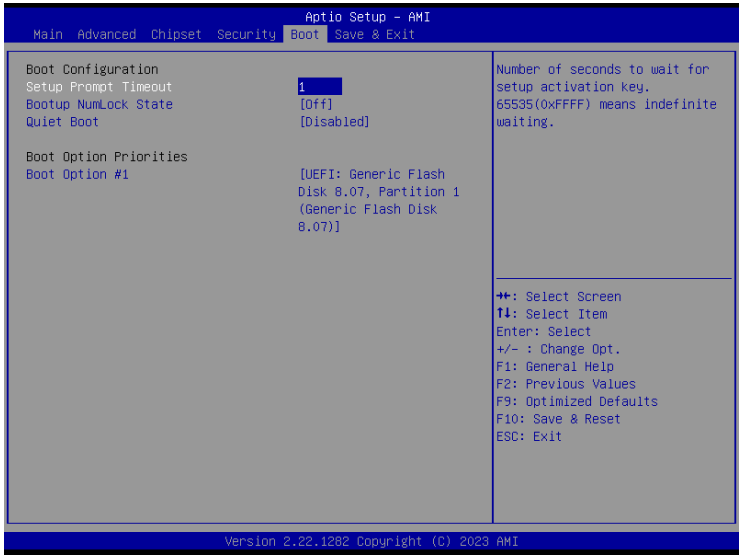
Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

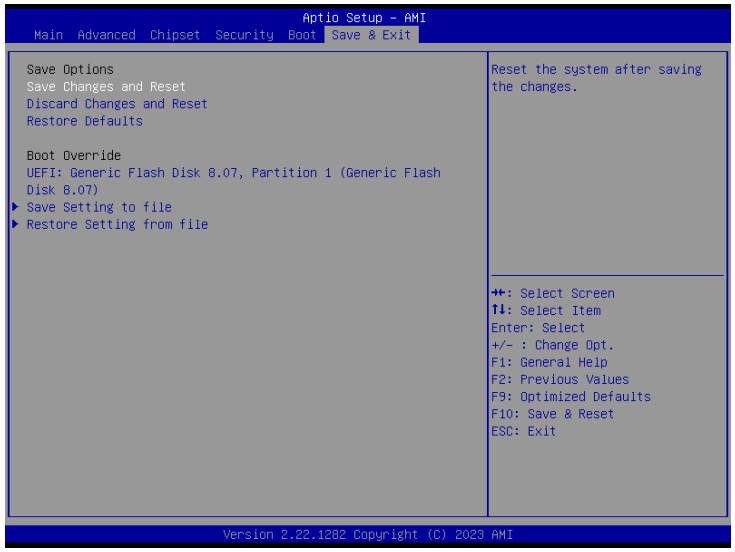
Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

► Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

► Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

▶ Notice: BIOS SPI ROM

- 1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

c. After updating unique MAC Address from manufacturing, NVM will be protected immediately after power cycle.
Users cannot update NVM or MAC address.