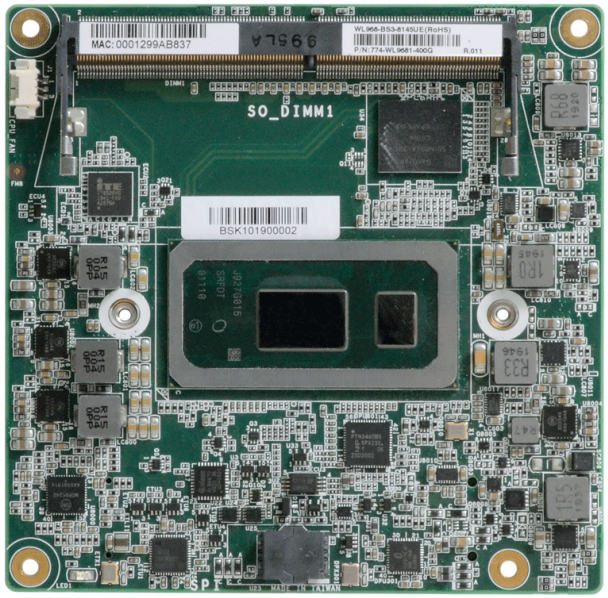
DFI®



WL968

COM Express Compact Module
User's Manual

A-617-M-2046

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Copyright

Trademarks

COM Express Specification Reference

PICMG® COM Express Module™ Base Specification.

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

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Warranty

1. Warranty does not cover damages or failures that occur from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

4. We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

2. Wear an antistatic wrist strap.

3. Do all preparation work on a static-free surface.

4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

To avoid damage to the system:
- Use the correct AC input voltage range.

To reduce the risk of electric shock:
- Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- 1 WL968 board
- 1 CPU Cooler (for -40 to 85°C, H=35.2mm): A71-108124-000G
- 1 Heat sink (for 0 to 60°C, H=26.8mm): A71-008151-000G

Optional Items

- COM332-B carrier board kit 770-CM3321-000G
- Heatspreader (H=11mm) A71-808324-000G

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

SYSTEM	Processor	8th Gen Intel® CoreTM Processor, FCBGA1528 Intel® Core™ i7-8665UE Processor, Quad Core, 8M Cache, 1.7GHz (4.4GHz), 15W Intel® Core™ i5-8365UE Processor, Quad Core, 6M Cache, 1.6GHz (4.1GHz), 15W Intel® Core™ i3-8145UE Processor, Dual Core, 4M Cache, 2.2GHz (3.9GHz), 15W Intel® Celeron® Processor 4305UE, Dual Core, 2M Cache, 2.0GHz (2.0GHz), 15W
	Memory	Two 260-pin SODIMM up to 64GB Dual Channel DDR4 2133MHz
	BIOS	AMI SPI 128Mbit
GRAPHICS	Controller	Intel® HD Graphics
	Feature	OpenGL 4.5, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H265, VP8, VP9 HW Encode: AVC/H.264, MPEG2, JPEG, HEVC/H265, VP8, VP9
	Display	1 x VGA/DDI (DDI available upon request) 1 x LVDS/eDP (eDP available upon request) 1 x DDI VGA: resolution up to 1920x1200 @ 60Hz LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz eDP: resolution up to 4096x2304 @ 60Hz HDMI: resolution up to 4096x2160 @ 30Hz DP++: resolution up to 4096x2304 @ 60Hz
	Triple Displays	VGA + LVDS + DDI DDI + eDP + DDI
EXPANSION	eMMC	1 x 8GB/16GB/32GB/64GB/128GB eMMC 5.1 (available upon request)
	Interface	6 PCIe x1 or 2 PCIe x1 + 1 PCIe x4 or 3 PCIe x1 + 2 PCIe x2 (support up to 5 devices and 7 lanes) 1 x LPC 1 x I2C 1 x SMBus 2 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I219LM with iAMT12.x PCIe (10/100/1000Mbps)
I/O	USB	4 x USB 3.0 8 x USB 2.0
	SATA	Default 2 x SATA , 3 x SATA by BOM request, SATA 3.0 (up to 6Gb/s) RAID 0/1/5
	DIO	1 x 8-bit DIO

WATCHDOG TIMER	Output & Interval	Support COM Express 3kinds WDT Modes by BIOS setting
SECURITY	TPM	Available Upon Request
POWER	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
	Consumption	TBD
OS SUPPORT		Windows: Windows 10 IoT Enterprise 64-bit Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C (For normal Temperature skus); -40 to 85°C (For Extend temperature skus with Heat spreader, Heat-sink and active Fan) Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
	MTBF	28W@25°C
MECHANICAL	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")
	Compliance	PICMG COM Express® R3.0, Type 6
Certifications	Certifications	CE, FCC, RoHS

Features

• Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

• DDR4

DDR4 delivers increased system bandwidth and improves performance. DDR4 improves the performance at a lower power than DDR3/DDR2.

• Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It delivers enhanced media conversion rates and higher frame rates on 4K Ultra HD videos. These enhancements deliver the performance and compatibility to meet the demand for business and home entertainment applications.

• Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 6Gb/s (SATA 3.0), it improves hard drive performance faster than the standard parallel ATA whose data transfer rate is 100MB/s. The bandwidth of the SATA 3.0 will be limited by carrier board design.

• Gigabit LAN

The Intel® I219LM Gigabit LAN PHY controller supports up to 1Gbps data transmission.

• USB

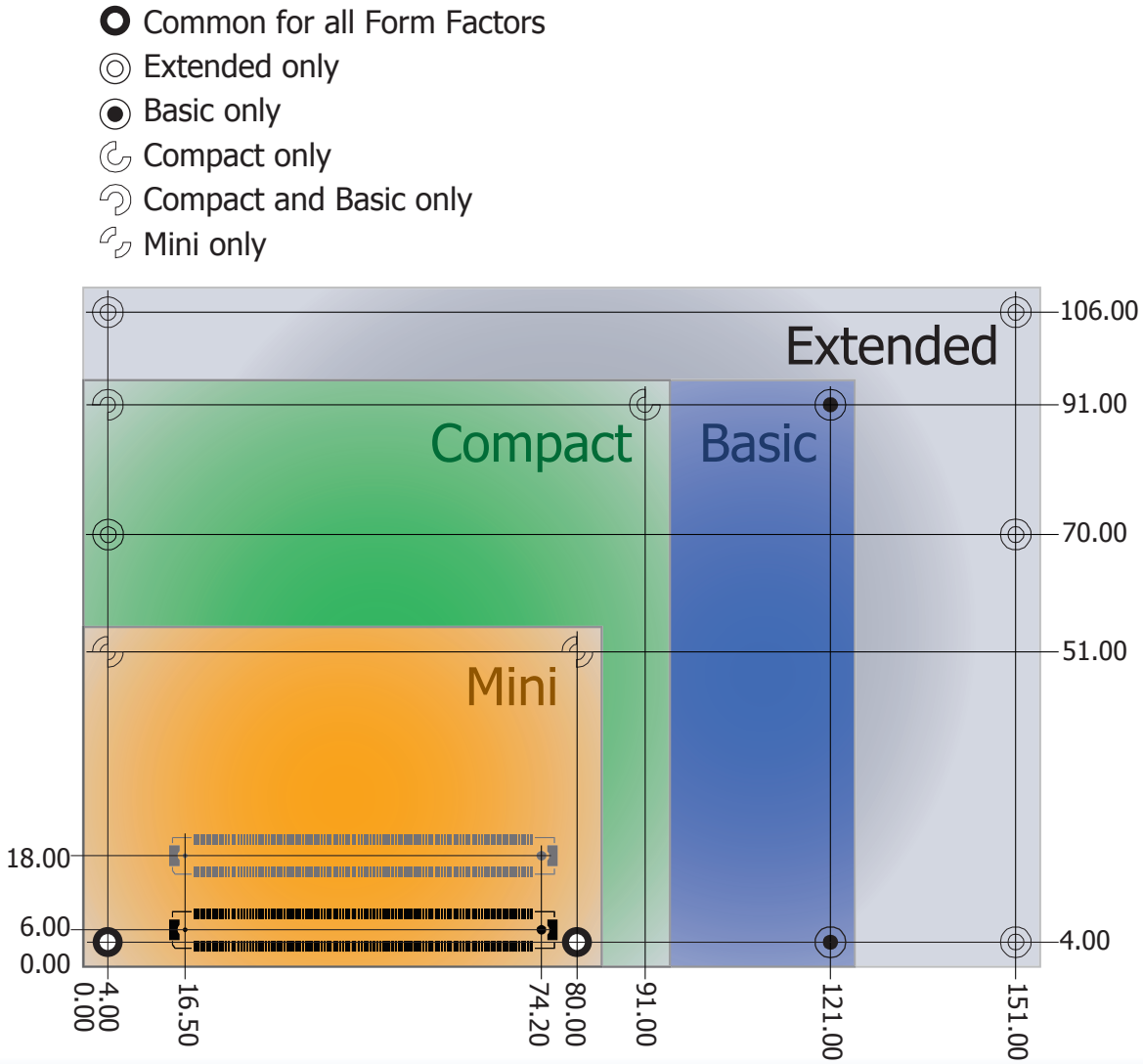
The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

Chapter 2 - Concept

COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

The dimension of COM Express Compact module is 95mm x 95mm.



Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the WL968 module.

Module Pin-out - Required and Optional Features A-B Connector. PICMG® COM.0 Revision 2.1

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI KU968 Type 6
A-B		System I/O	
A-B	PCI Express Lanes 0 - 5	1 / 6	6
A-B	LVDS Channel A	0 / 1	1
A-B	LVDS Channel B	0 / 1	1
A-B	eDP on LVDS CH A pins	0 / 1	1
A-B	VGA Port	0 / 1	0/1 (Option : DDI2 or VGA)
A-B	TV-Out	NA	NA
A-B	DDI 0	NA	NA
A-B[1]	Serial Ports 1 - 2	0 / 2	2
A-B	CAN interface on SER1	0 / 1	0
A-B	SATA / SAS Ports	1 / 4	Default 2xSATA
A-B	AC'97 / HDA Digital Interface	0 / 1	1
A-B	USB 2.0 Ports	4 / 8	8
A-B	USB Client	0 / 1	0
A-B	USB 3.0 Ports	NA	NA
A-B	LAN Port 0	1 / 1	1
A-B	LPC Bus	1 / 1	1
A-B	SPI	1 / 2	1
A-B	System Management		
A-B[2]	SDIO (muxed on GPIO)	0 / 1	0
	General Purpose I/O	8 / 8	8
A-B	SMBus	1 / 1	1
A-B	I2C	1 / 1	1
A-B	Watchdog Timer	0 / 1	1
A-B	Speaker Out	1 / 1	1
A-B	External BIOS ROM Support	0 / 2	1
A-B	Reset Functions	1 / 1	1
A-B	Power Management		
A-B	Thermal Protection	0 / 1	1
A-B	Battery Low Alarm	0 / 1	1
A-B	Suspend/Wake Signals	0 / 3	1
A-B	Power Button Support	1 / 1	1
A-B	Power Good	1 / 1	1
A-B	VCC_5V_SBY Contacts	4 / 4	4
A-B[1]	Sleep Input	0 / 1	1
A-B[1]	Lid Input	0 / 1	1
A-B[1]	Fan Control Signals	0 / 2	2
A-B	Trusted Platform Modules	0 / 1	1
A-B	Power		
A-B	VCC_12V Contacts	12 / 12	12

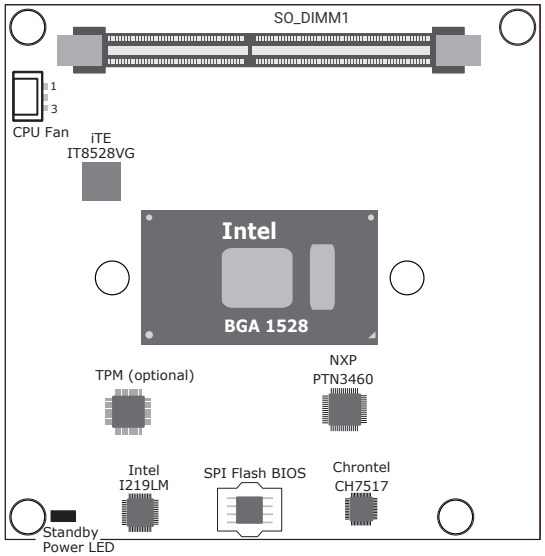
Module Pin-out - Required and Optional Features C-D Connector. PICMG® COM.0 Revision 2.1

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI KU968 Type 6
C-D	System I/O		
C-D[2]	PCI Express Lanes 16 - 31	0 / 16	0
	PCI Express Graphics (PEG)	0 / 1	0
	Muxed SDVO Channels 1 - 2	NA	NA
C-D[2]	PCI Express Lanes 6 - 15	0 / 2	Default 1 , 2 by BOM request
	PCI Bus - 32 Bit	NA	NA
	PATA Port	NA	NA
	LAN Ports 1 - 2	NA	NA
	DDIs 1 - 3	0 / 3	1/2 (Option : DDI2 or VGA)
	USB 3.0 Ports	0 / 4	4
C-D	Power		
C-D	VCC_12V Contacts	12 / 12	12

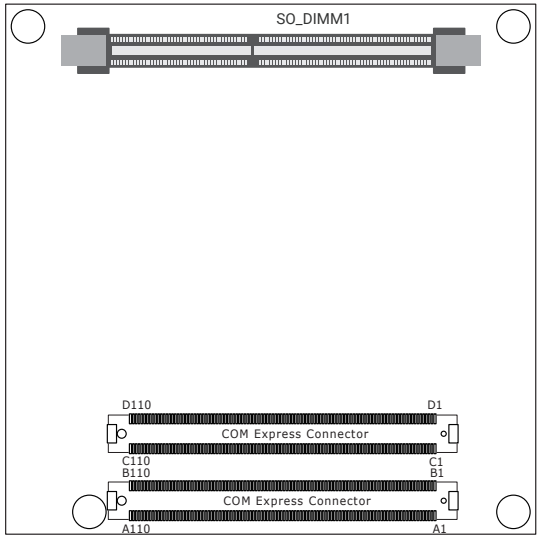
- 1 Indicates 12V-tolerant features on former VCC_12V signals.
- 2 Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

Chapter 3 - Hardware Installation

Board Layout



Top View



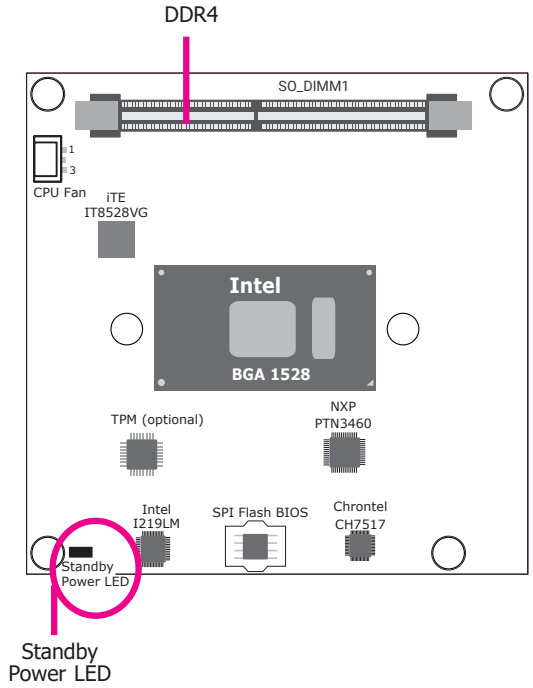
Bottom View

Important:
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

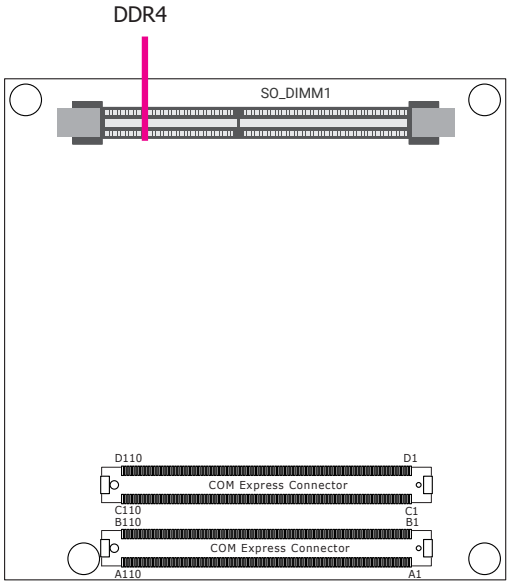
System Memory

The system board is equipped with Two 260-pin SODIMM up to 64GB Dual Channel DDR4 memory onboard supporting 2400MHz, dual channel memory interface.

Important:
When the Standby Power LED is red, it indicates that there is power on the board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



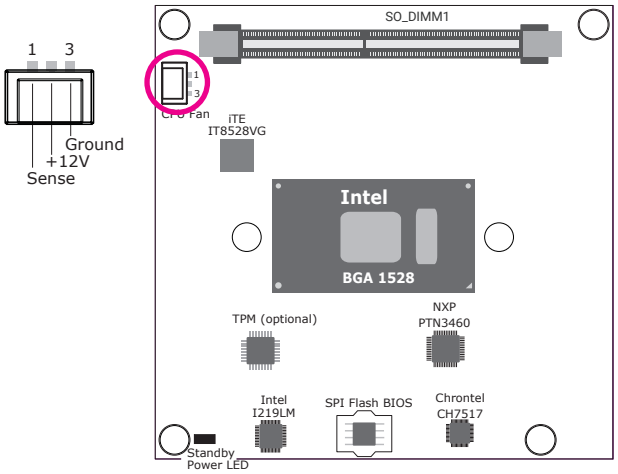
Top View



Bottom View

Connectors

CPU Fan Connector



Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

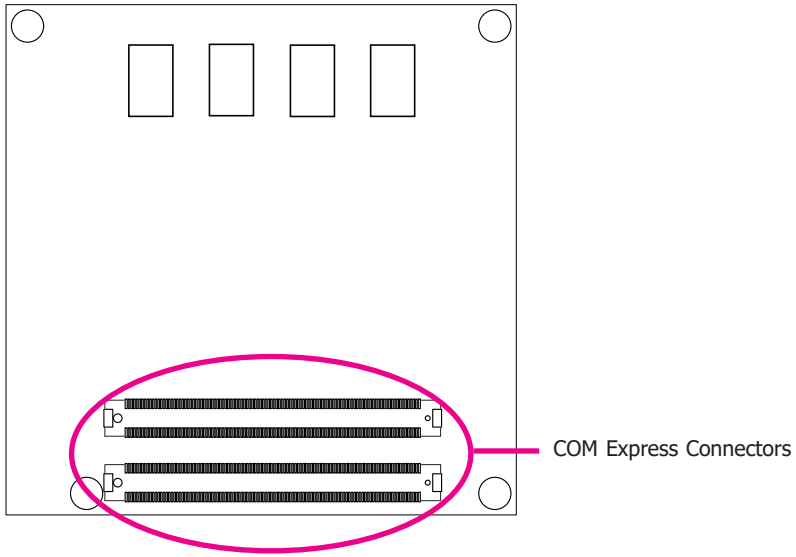
BIOS Setting

"PC Health Status" submenu in the Advanced menu of the BIOS will display the current speed of the cooling fan.

COM Express Connectors

The COM Express connectors are used to interface the WL968 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.

Refer to the "Installing WL968 onto a Carrier Board" section for more information.



Refer to the following pages for the pin functions of these connectors.

COM Express Connectors

Row A		Row B		Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	LVDS_B0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	LVDS_B1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	NA	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	NA	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	NA	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	NA	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	NA	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA _SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA _RST#	B30	AC/HDA _SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA _BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA _SDOUT	B33	I2C_CK	A88	PCIE0_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CLK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	NA	A102	SER1_RX	B102	FAN_TACHIN
A48	NA	B48	NA	A103	LID#	B103	SLEEP#
A49	NA	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)

Row C		Row D		Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)	C56	NA	D56	NA
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	NA	D58	NA
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	NA	D59	NA
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	NA	D61	NA
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	NA	D62	NA
C8	GND	D8	GND	C63	RSVD	D63	RSVD
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	RSVD
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	NA	D65	NA
C11	GND (FIXED)	D11	GND (FIXED)	C66	NA	D66	NA
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RAPID_SHUTDOWN	D67	GND
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	NA	D68	NA
C14	GND	D14	GND	C69	NA	D69	NA
C15	NA	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)
C16	NA	D16	DDI1_CTRLDATA_AUX-	C71	NA	D71	NA
C17	RSVD	D17	RSVD	C72	NA	D72	NA
C18	RSVD	D18	RSVD	C73	GND	D73	GND
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	NA	D74	NA
C20	PCIE_RX6-	D20	PCIE_TX6-	C75	NA	D75	NA
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND
C22	PCIE_RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD
C23	PCIE_RX7-	D23	PCIE_TX7-	C78	NA	D78	NA
C24	DDI1_HPD	D24	RSVD	C79	NA	D79	NA
C25	NA	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)
C26	NA	D26	DDI1_PAIR0+	C81	NA	D81	NA
C27	RSVD	D27	DDI1_PAIR0-	C82	NA	D82	NA
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD
C29	NA	D29	DDI1_PAIR1+	C84	GND	D84	GND
C30	NA	D30	DDI1_PAIR1-	C85	NA	D85	NA
C31	GND (FIXED)	D31	GND (FIXED)	C86	NA	D86	NA
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+	C87	GND	D87	GND
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-	C88	NA	D88	NA
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	NA	D89	NA
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)
C36	NA	D36	DDI1_PAIR3+	C91	NA	D91	NA
C37	NA	D37	DDI1_PAIR3-	C92	NA	D92	NA
C38	NA	D38	RSVD	C93	GND	D93	GND
C39	NA	D39	DDI2_PAIR0+	C94	NA	D94	NA
C40	NA	D40	DDI2_PAIR0-	C95	NA	D95	NA
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND
C42	NA	D42	DDI2_PAIR1+	C97	RSVD	D97	RSVD
C43	NA	D43	DDI2_PAIR1-	C98	NA	D98	NA
C44	NA	D44	DDI2_HPD	C99	NA	D99	NA
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)
C46	NA	D46	DDI2_PAIR2+	C101	NA	D101	NA
C47	NA	D47	DDI2_PAIR2-	C102	NA	D102	NA
C48	RSVD	D48	RSVD	C103	GND	D103	GND
C49	NA	D49	DDI2_PAIR3+	C104	VCC_12V	D104	VCC_12V
C50	NA	D50	DDI2_PAIR3-	C105	VCC_12V	D105	VCC_12V
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC_12V
C52	NA	D52	NA	C107	VCC_12V	D107	VCC_12V
C53	NA	D53	NA	C108	VCC_12V	D108	VCC_12V
C54	TYPE0#	D54	PEG_LANE_RV#	C109	VCC_12V	D109	VCC_12V
C55	NA	D55	NA	C110	GND (FIXED)	D110	GND (FIXED)

COM Express Connectors Signals and Descriptions

Pin Types
I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output

AC97/HDA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
AC/HDA_RST#	A30	O CMOS	3.3V Suspend/3.3V		Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V		Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V		Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
AC/HDA_SDOUT	A33	O CMOS	3.3V/3.3V		Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	NA		Serial TDM data inputs from up to 2 CODECs.
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V			
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN	

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-	
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-	
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-	
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and **recommend** current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.

SATA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	NA	Default NA (Request by BOM option)	Serial ATA or SAS Channel 2 transmit differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	NA		
SATA2_RX+	A25	I SATA	AC coupled on Module	NA	Default NA (Request by BOM option)	Serial ATA or SAS Channel 2 receive differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	NA		
SATA3_TX+	B22	O SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 transmit differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	NA		
SATA3_RX+	B25	I SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 receive differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	NA		
(S)ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	Connect to LED and **recommend** current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

PCI Express Lanes Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69			AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 1
PCIE_TX1-	A65			AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 1
PCIE_RX1-	B65					

PCI Express Lanes Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 2
PCIE_TX2-	A62			AC Coupling capacitor		
PCIE_RX2+	B61	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 2
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 3
PCIE_TX3-	A59			AC Coupling capacitor		
PCIE_RX3+	B58	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 3
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 4
PCIE_TX4-	A56			AC Coupling capacitor		
PCIE_RX4+	B55	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 4
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 5
PCIE_TX5-	A53			AC Coupling capacitor		
PCIE_RX5+	B52	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 5
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 6
PCIE_TX6-	D20			AC Coupling capacitor		
PCIE_RX6+	C19	I PCIE	AC coupled off Module		**Device** - Connect AC Coupling cap 0.1uF **Slot** - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 6
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module	NA	Default NA(Request by BOM option)	PCI Express Differential Transmit Pairs 7
NA	NA			NA		
PCIE_RX7+	C22	I PCIE	AC coupled off Module		Default NA(Request by BOM option)	PCI Express Differential Receive Pairs 7
PCIE_RX7-	C23					
PCIE0_CLK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, **PCIe CLK Buffer** or slot	Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE0_CLK_REF-	A89					

PEG Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
PEG_TX0+	D52	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 0
PEG_TX0-	D53			NA		
PEG_RX0+	C52	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 0
PEG_RX0-	C53			NA		
PEG_TX1+	D55	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 1
PEG_TX1-	D56			NA		
PEG_RX1+	C55	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 1
PEG_RX1-	C56			NA		
PEG_TX2+	D58	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 2
PEG_TX2-	D59			NA		
PEG_RX2+	C58	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 2
PEG_RX2-	C59			NA		
PEG_TX3+	D61	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 3
PEG_TX3-	D62			NA		
PEG_RX3+	C61	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 3
PEG_RX3-	C62			NA		
PEG_TX4+	D65	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 4
PEG_TX4-	D66			NA		
PEG_RX4+	C65	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 4
PEG_RX4-	C66			NA		
PEG_TX5+	D68	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 5
PEG_TX5-	D69			NA		
PEG_RX5+	C68	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 5
PEG_RX5-	C69			NA		
PEG_TX6+	D71	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 6
PEG_TX6-	D72			NA		
PEG_RX6+	C71	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 6
PEG_RX6-	C72			NA		
PEG_TX7+	D74	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 7
PEG_TX7-	D75			NA		
PEG_RX7+	C74	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 7
PEG_RX7-	C75			NA		
PEG_TX8+	D78	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 8
PEG_TX8-	D79			NA		
PEG_RX8+	C78	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 8
PEG_RX8-	C79			NA		
PEG_TX9+	D81	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 9
PEG_TX9-	D82			NA		
PEG_RX9+	C81	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 9
PEG_RX9-	C82			NA		
PEG_TX10+	D85	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 10
PEG_TX10-	D86			NA		
PEG_RX10+	C85	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 10
PEG_RX10-	C86			NA		
PEG_TX11+	D88	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 11
PEG_TX11-	D89			NA		
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89			NA		

PEG Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
PEG_TX12+	D91	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 12
PEG_TX12-	D92			NA		
PEG_RX12+	C91	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 12
PEG_RX12-	C92			NA		
PEG_TX13+	D94	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 13
PEG_TX13-	D95			NA		
PEG_RX13+	C94	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 13
PEG_RX13-	C95			NA		
PEG_TX14+	D98	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 14
PEG_TX14-	D99			NA		
PEG_RX14+	C98	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 14
PEG_RX14-	C99			NA		
PEG_TX15+	D101	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102			NA		
PEG_RX15+	C101	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 15
PEG_RX15-	C102			NA		
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.

DDI Signals Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
DDI1_PAIR0+/SDVO1_RED+	D26	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI1_PAIR0-/SDVO1_RED-	D27				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1+/SDVO1_GRN+	D29	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI1_PAIR1-/SDVO1_GRN-	D30				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR2+/SDVO1_BLU+	D32	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI1_PAIR2-/SDVO1_BLU-	D33				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR3+/SDVO1_CK+	D36	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair
DDI1_PAIR3-/SDVO1_CK-	D37				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR4+/SDVO1_INT+	C25	I PCIE	AC coupled off Module	NA		Serial Digital Video B interrupt input differential pair.
DDI1_PAIR4-/SDVO1_INT-	C26			NA		
DDI1_PAIR5+/SDVO1_TVCLKIN+	C29	I PCIE	AC coupled off Module	NA		Serial Digital Video TVOUT synchronization clock input differential pair.
DDI1_PAIR5-/SDVO1_TVCLKIN-	C30			NA		
DDI1_PAIR6+/SDVO1_FLDSTALL+	C15	I PCIE	AC coupled off Module	NA		Serial Digital Video Field Stall input differential pair.
DDI1_PAIR6-/SDVO1_FLDSTALL-	C16			NA		
DDI1_CTRLCLK_AUX+/SDVO1_CTRLCLK	D15	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
DDI1_CTRLDATA_AUX-/SDVO1_CTRLDATA	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V/PU 100K to 3.3V **(S/W IC between 4.7K/100K resistor)**	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
DDI1_HPD	C24	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI2_PAIR0+	D39	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 0 differential pairs
DDI2_PAIR0-	D40				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR1+	D42	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 1 differential pairs
DDI2_PAIR1-	D43			DDI2 is option function	Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 2 differential pairs
DDI2_PAIR2-	D47				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_PAIR3+	D49	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 3 differential pairs
DDI2_PAIR3-	D50				Connect AC Coupling Capacitors 0.1uF to Device	
DDI2_CTRLCLK_AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND **(S/W IC between Rpu/PCH)**	Connect to DP AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)**	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
DDI2_CTRLDATA_AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V **(S/W IC between Rpu/PCH)**	Connect to DP AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V/PU 100K to 3.3V **(S/W IC between 4.7K/100K resistor)**	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high
DDI2_HPD	D44	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

DDI3_PAIR0+	C39	O PCIE	AC coupled off Module	NA		DDI 3 Pair 0 differential pairs
DDI3_PAIR0-	C40			NA		
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module	NA		DDI 3 Pair 1 differential pairs
DDI3_PAIR1-	C43			NA		
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module	NA		DDI 3 Pair 2 differential pairs
DDI3_PAIR2-	C47			NA		
DDI3_PAIR3+	C49	O PCIE	AC coupled off Module	NA		DDI 3 Pair 3 differential pairs
DDI3_PAIR3-	C50			NA		
DDI3_CTRLCLK_AUX+	C36	I/O PCIE	AC coupled on Module	NA		DP AUX+ function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high
DDI3_CTRLDATA_AUX-	C37	I/O PCIE	AC coupled on Module	NA		DP AUX- function if DDI3_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high
DDI3_HPD	C44	I CMOS	3.3V / 3.3V	NA		DDI Hot-Plug Detect
DDI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	NA		Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

USB Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 3
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 4
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.3V		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 7
USB7-	B36					
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	D4	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	D3			AC Coupling capacitor		
USB_SSRX0+	C4	I PCIE	AC coupled off Module		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	C3					
USB_SSTX1+	D7	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	D6			AC Coupling capacitor		
USB_SSRX1+	C7	I PCIE	AC coupled off Module		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	C6					
USB_SSTX2+	D10	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX2-	D9			AC Coupling capacitor		
USB_SSRX2+	C10	I PCIE	AC coupled off Module		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9					
USB_SSTX3+	D13	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3-	D12			AC Coupling capacitor		
USB_SSRX3+	C13	I PCIE	AC coupled off Module		Connect 90☒ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX3-	C12					

LVDS Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
LVDS_A0+	A71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A0-	A72					
LVDS_A1+	A73	O LVDS	LVDS		Connect to LVDS connector	

LVDS_A1-	A74					on-board
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79					
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82					
LVDS_B0+	B71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board
LVDS_B0-	B72					
LVDS_B1+	B73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B1-	B74					
LVDS_B2+	B75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B2-	B76					
LVDS_B3+	B77	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B3-	B78					
LVDS_B_CK+	B81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel B differential clock
LVDS_B_CK-	B82					
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel power circuit	LVDS panel power enable
LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V		Connect to brightness control of LVDS panel backlight power circuit.	LVDS panel backlight brightness control
LVDS_I2C_CK	A83	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC clock of LVDS panel	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC data of LVDS panel	I2C data line for LVDS display use

LPC Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
LPC_AD0	B4	I/O CMOS	3.3V / 3.3V		Connect to LPC device	LPC multiplexed address, command and data bus
LPC_AD1	B5					
LPC_AD2	B6					
LPC_AD3	B7					
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V			LPC frame indicates the start of an LPC cycle
LPC_DRQ0#	B8	I CMOS	3.3V / 3.3V	PU 10K to 3.3V	NC	LPC serial DMA request
LPC_DRQ1#	B9			PU 10K to 3.3V	NC	
LPC_SERIRQ	A50	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	Connect to LPC device	LPC serial interrupt
LPC_CLK	B10	O CMOS	3.3V / 3.3V			LPC clock output - 24MHz nominal

SPI Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V		**Connect to Carrier Board SPI Device CS# pin**	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V		**Connect a series resistor 33Ω to Carrier Board SPI Device SO pin**	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V		**Connect a series resistor 33Ω to Carrier Board SPI Device SI pin**	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		**Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin**	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V			Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.
BIOS_DIS0#	A34	I CMOS	NA			Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to below table for strapping options of BIOS disable signals.
BIOS_DIS1#	B88					

BIOS DIS1#	BIOS DIS0#	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	Bios Entry	Ref Line
1	**1**	Module	Module	High	Module	SPI0/SPI1	0
1	**0**	Module	Module	High	Module	Carrier FWH	1
0	**1**	Module	Carrier	SPI0	Carrier	SPI0/SPI1	2
0	**0**	**Carrier (Default)**	**Module (Default)**	**SPI1 (Default)**	**Module (Default)**	**SPI0/SPI1 (Default)**	**3**

VGA Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
VGA_RED	B89	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Red for monitor. Analog output
VGA_GRN	B91	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Green for monitor. Analog output
VGA_BLU	B92	O Analog	Analog	PD 150 to GND	**PD 150R,connect to VGA connector with EMI filter & ESD protect component.**	Blue for monitor. Analog output
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		**Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device**	Horizontal sync output to VGA monitor

VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		**Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display Device**	Vertical sync output to VGA monitor
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	**Connect to VGA connector with a 3.3V to 5V Level shift circuit.**	DDC data line.

Serial Interface Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
SER0_TX	A98	O CMOS	3.3V/5V		PD 4.7K to GND	General purpose serial port 0 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER0_RX	A99	I CMOS	3.3V/5V	PU 10K to 3.3V		General purpose serial port 0 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_TX	A101	O CMOS	3.3V/5V		PD 4.7K to GND	General purpose serial port 1 transmitter **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SER1_RX	A102	I CMOS	3.3V/5V	PU 10K to 3.3V		General purpose serial port 1 receiver **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**

Miscellaneous Signal Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		General purpose I2C port data I/O line
SPKR	B32	O CMOS	3.3V / 3.3V			Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.
FAN_PWMOUT	B101	O OD CMOS	3.3V / 3.3V			Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
FAN_TACHIN	B102	I OD CMOS	3.3V / 3.3V	PU 47K to 3V3		Fan tachometer input for a fan with a two pulse output. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
TPM_PP	A96	I CMOS	3.3V / 3.3V	Default NA, PD 4.7K when stuff TPM chip		Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.

Power and System Management Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU	NC PU 4.7K to 3V3_SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V	PD 100K to GND		Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10K to 5V and PD 20K		Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V			Indicates imminent suspend operation; used to notify LPC devices.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 10K to GND		Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 1K to 3V3_DU		PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU		General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3V3_DU		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3_DU_EC		LID switch. Low active signal used by the ACPI operating system for a LID switch. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 10K to 3V3_DU_EC		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. **(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)**
THRM#	B35	I CMOS	3.3V / 3.3V	PU 10K to 3V3		Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional clock line.

SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU	NC PU 4.7K to 3V3_SB	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

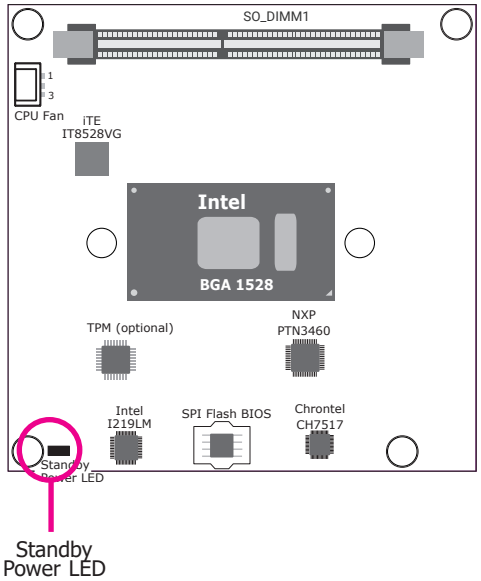
GPIO Signals Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins. **Upon a hardware reset, these outputs should be low.**
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		General purpose input pins. **Pulled high internally on the Module.**
GPI1	A63			PU 10K to 3.3V		
GPI2	A67			PU 10K to 3.3V		
GPI3	A85			PU 10K to 3.3V		

Power and GND Signal Descriptions

Signal	Pin#	Module Pin Type	Pwr Rail / Tolerance	WL968	Carrier Board	Description
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.
VCC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.
GND	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.

Standby Power LED



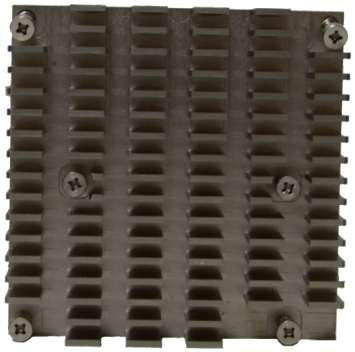
This LED will be lit when the system is in standby mode.

1

Cooling Option

Heat Sink

Note:
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.



Top View of the Heat Sink

Bottom View of the Heat Sink

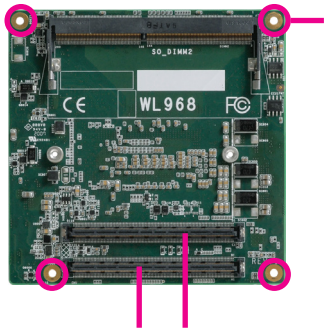
• "1" denotes the location of the thermal pad designed to contact the corresponding components that are on the WL968.

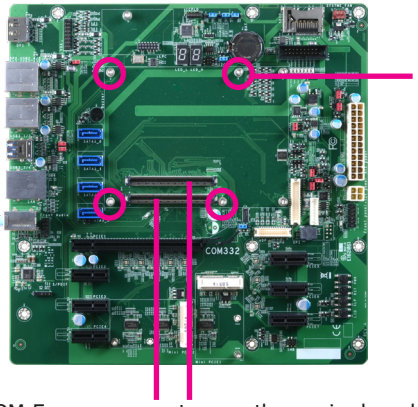
Important:
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto the WL968.

Installing WL968 onto a Carrier Board

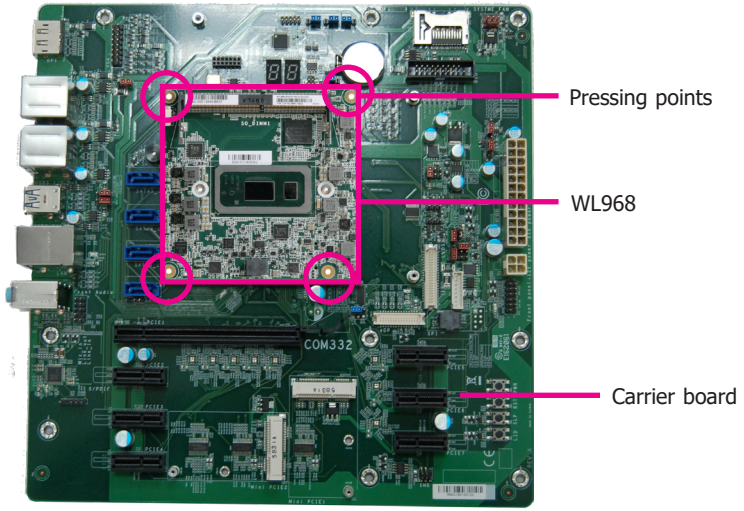
Important:
The carrier board (COM332-B) and COM Express module used in this section are for reference purpose only and may not resemble you carrier board and the acutal WL968 module. These illustrations are mainly to guide you on how to install WL968 onto the carrier board of your choice.

1. Grasp WL968 by its edges and position it on top of the carrier board with the mounting holes of WL968 aligning with the standoffs on the carrier board. This will also align the COM Express connectors of the two boards to each other.



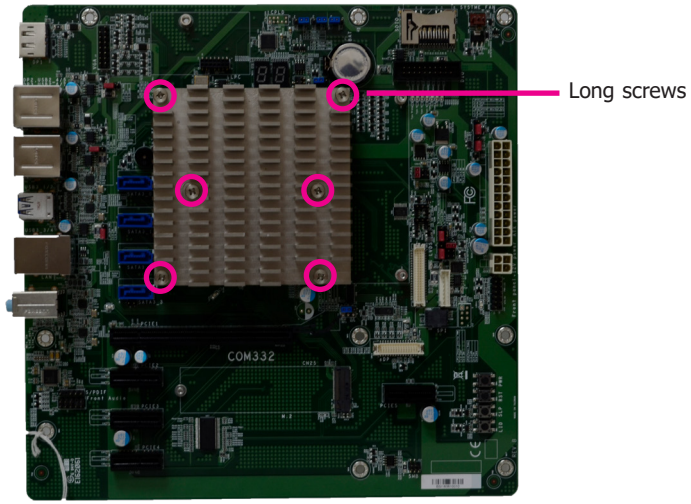


2. Press WL968 down firmly to seat it in the COM Express connectors of the carrier board.



Note:
The illustration above shows the pressing points of the module onto the carrier board. Be careful when pressing the module to avoid damages to the connectors.

3. Use the provided mounting screws to secure WL968 with heat sink to the carrie board. The photo below shows the locations of the long mounting screws.

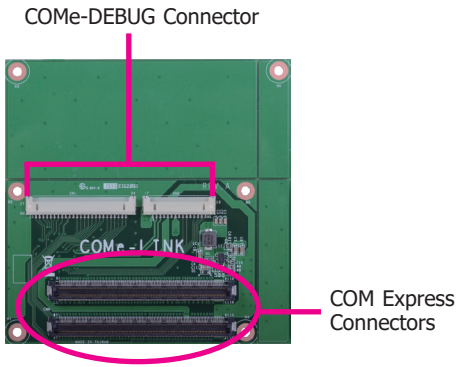


Installing the COM Express Debug Card (Optional)

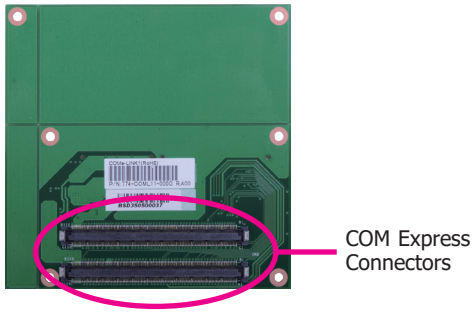
Note:
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

1. COMe-LINK1 is the COM Express debug card designed for COM Express Compact modules to debug and display signals and codes of COM Express modules.

COMe-LINK1



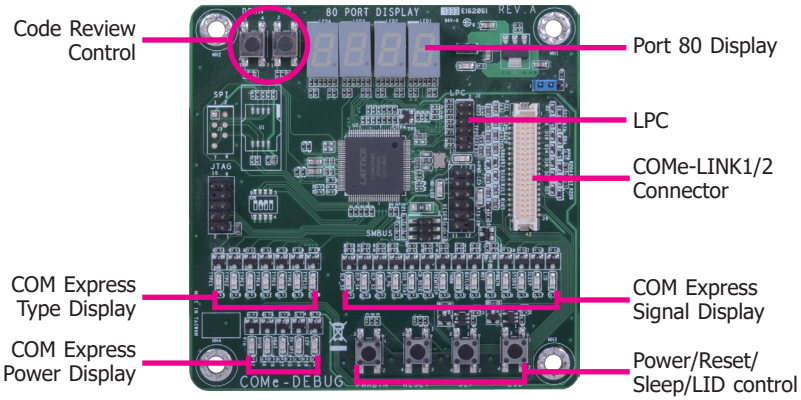
Top view

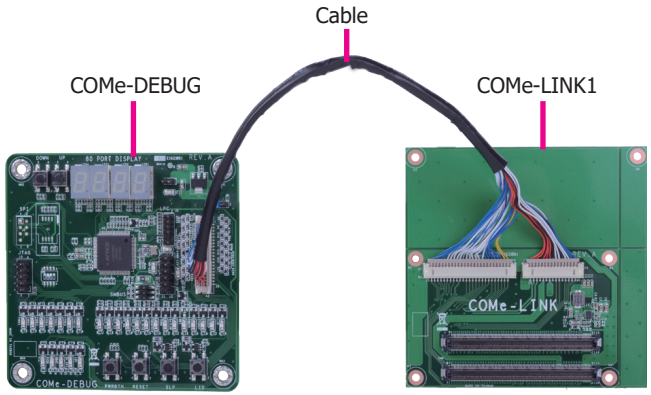


Bottom view

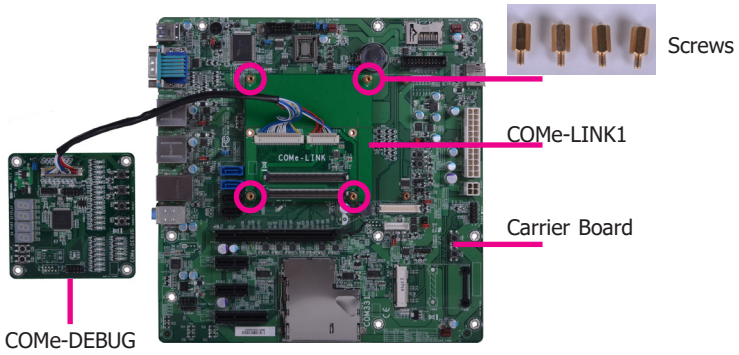
2. Connect the COMe-DEBUG card to COMe-LINK1 via a cable.

COMe-DEBUG

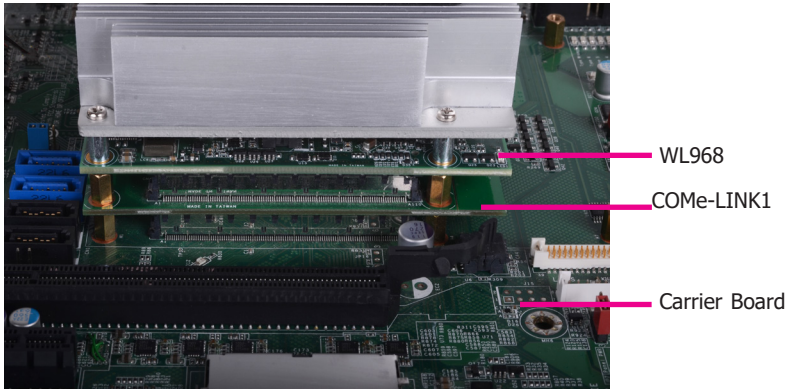




3. Use the provided screws to fix the COMe-LINK1 debug card onto the carrier board.



4. Then use the instructions from the previous section to install SU968 and heat sink on the top of the COMe-LINK1 debug card.



Side View of the Module, Debug Card and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu
Up and Down Arrows	Moves the highlight up or down between submenus or fields
<Esc>	Exits to the BIOS setup utility
<F1>	Displays general help
<F5/F6>	Changes the highlighted value
<F9>	Changes to the default setup
<F10>	Saves and exits the setup program.
<Enter>	Press <Enter> to enter the highlighted submenu.

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

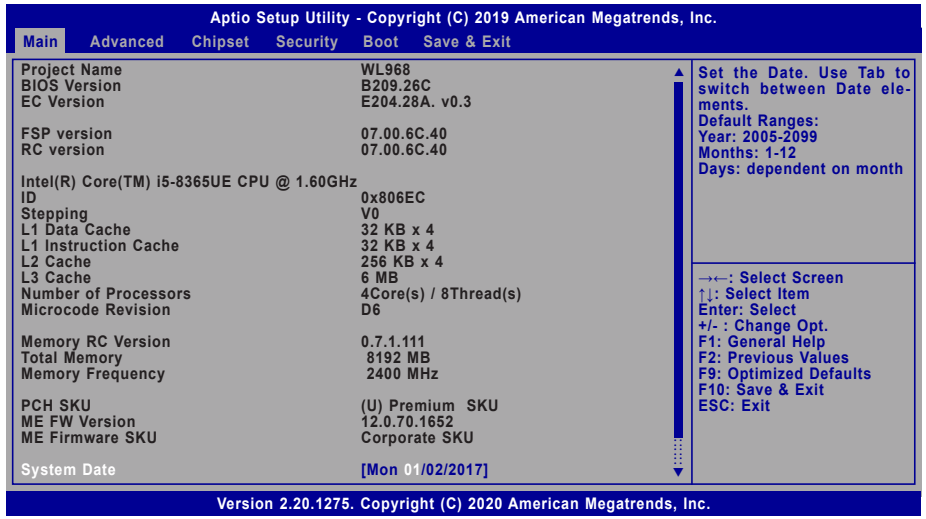
Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

Insyde BIOS Setup Utility

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <week>, <month>, <date>, <year>. Week displays the week, from Sun to Sat. Month displays the month, from 01 to 12. Date displays the date, from 01 to 31. Year displays the year, from 2000 to 2099.

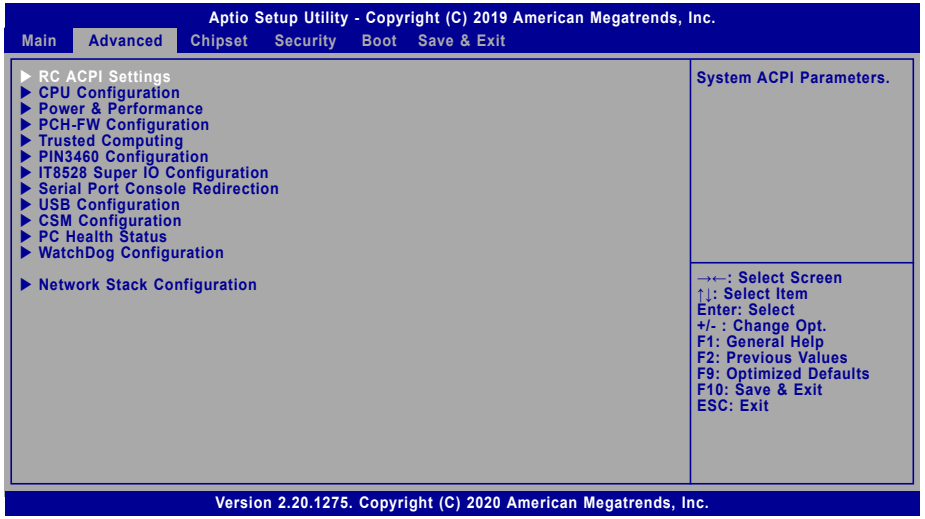
System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

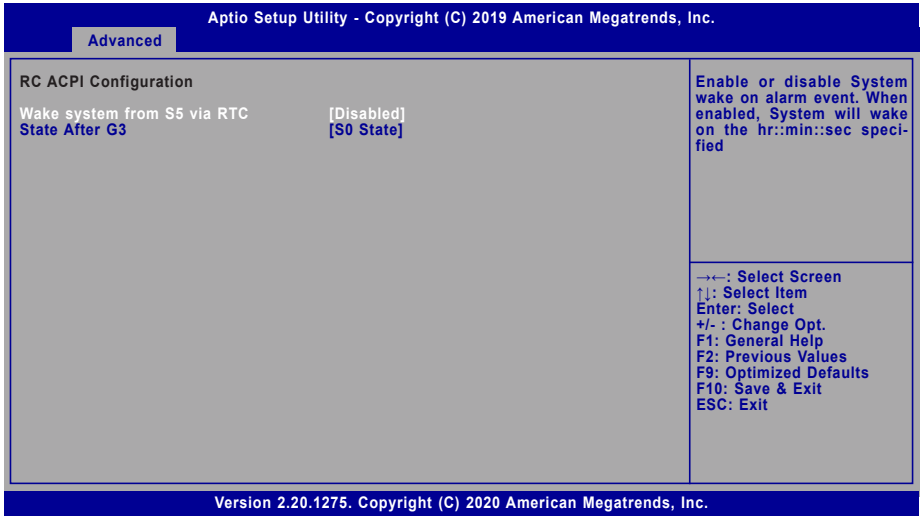
Advanced

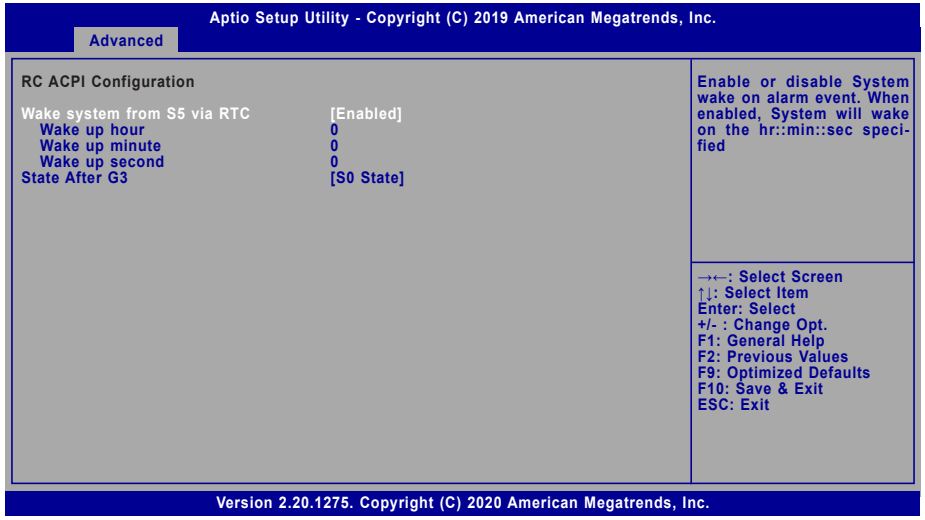
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



ACPI Configuration





Wake System from S5 via RTC

When Enabled, the system will automatically power up at a designated time every day. Once it's switched to [Enabled], please set up the time of day — hour, minute, and second — for the system to wake up.

State After G3

Select between S0 State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

S0 State The system automatically powers on after power failure.

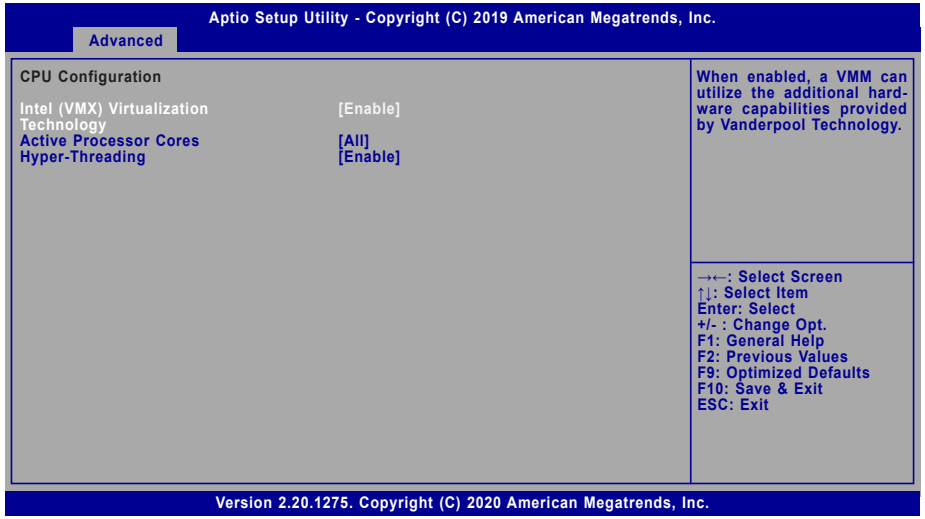
S5 State The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

Last State The system returns to the last state right before power failure.

Wake up time

When Wake On RTC is set to enabled, specify the wake up time of the day: <hour> (00~23), <minute> (00~59), <second> (00~59).

CPU Configuration



Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

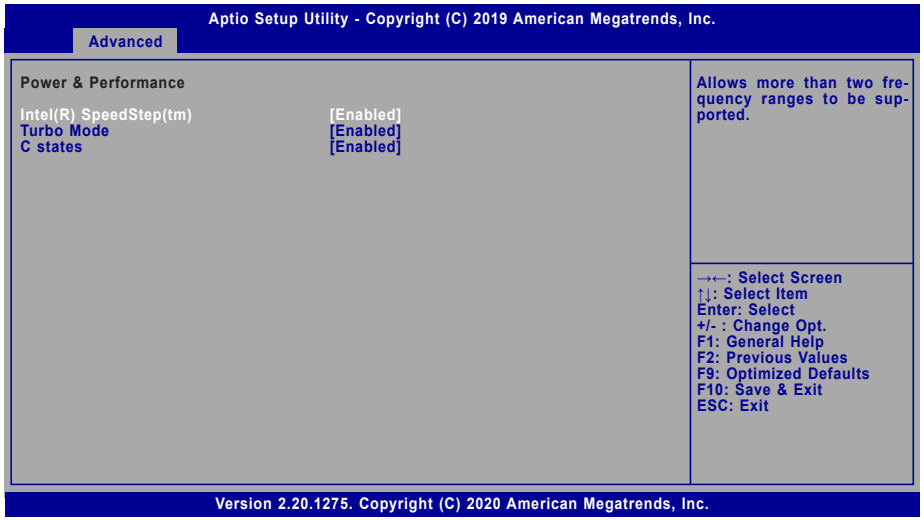
Select number of cores to enable in each processor package: all or 1.

Hyper-Threading

Enables this field for Windows and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

Note:
Some of the fields may not be available when the features are not supported by the equipped CPU.

Power & Performance



Intel(R) SpeedStep(tm)

This field is used to enable or disable the Intel SpeedStep® Technology, which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

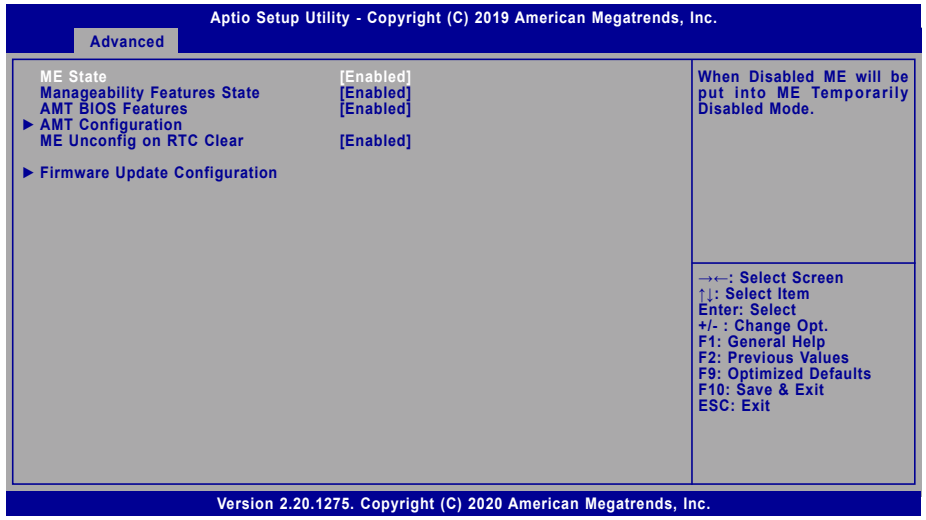
Turbo Mode

Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

C States

Enable or disable CPU Power Management. It allows CPU to enter "C states" when it's idle and nothing is executing.

PCH-FW Configuration



ME State

When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode.

Manageability Features State

Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

AMT BIOS Features

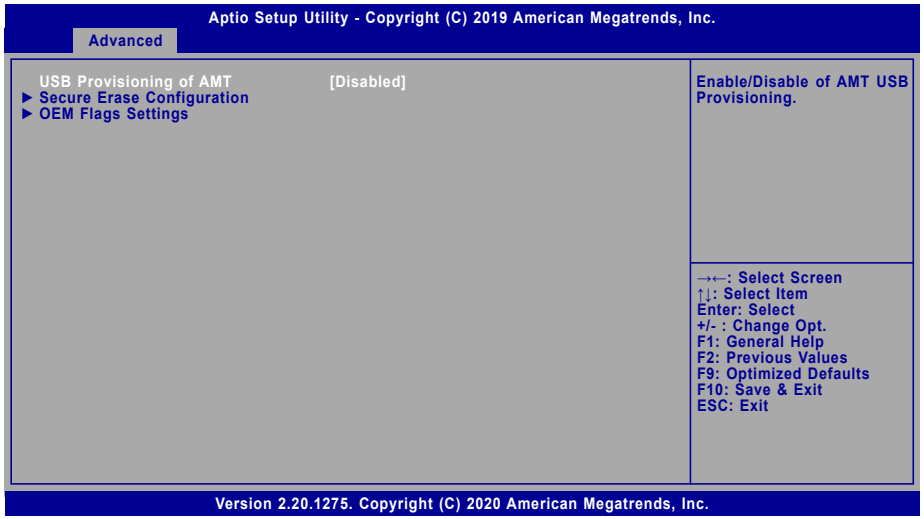
When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

ME Unconfig on RTC Clear

When disabled, ME will not be unconfigured on RTC Clear.

Note:
The sub-menus are detailed in following sections.

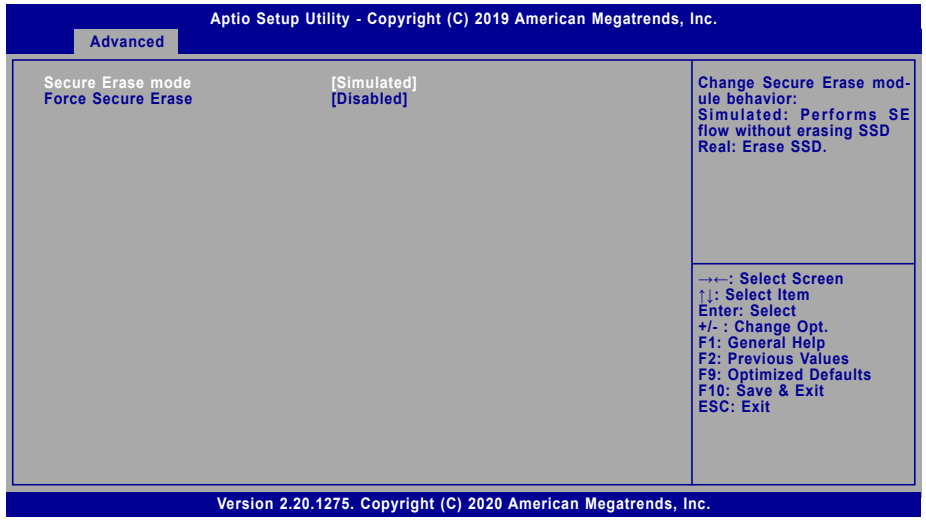
AMT Confuguration



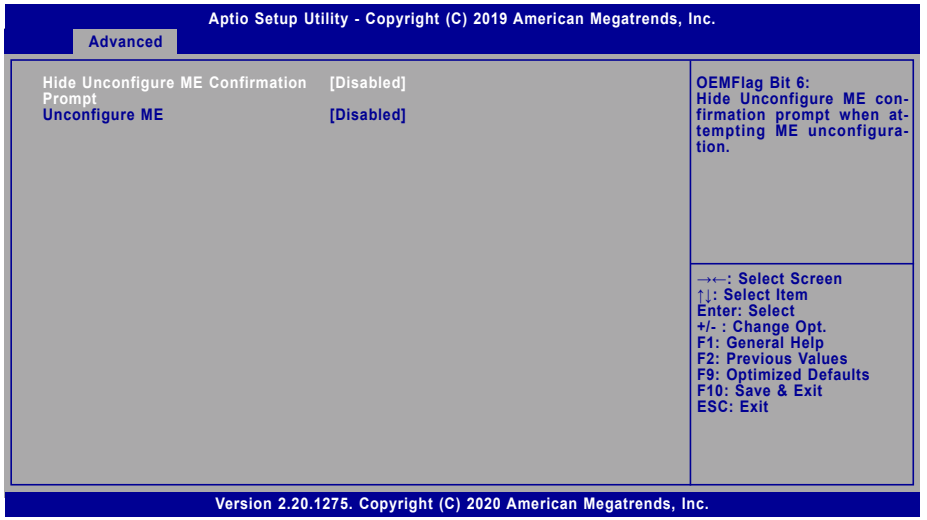
USB Provisioning of AMT

Enable or disable AMT USB Provisioning.

AMT Confuguration - Secure Erase Configuration



AMT Confuguration - OEM Flags Settings



Secure Erase Mode

Select Secure Erase module behavior: Simulated or Real.

Force Secure Erase

Enable or disable Force Secure Erase on next boot.

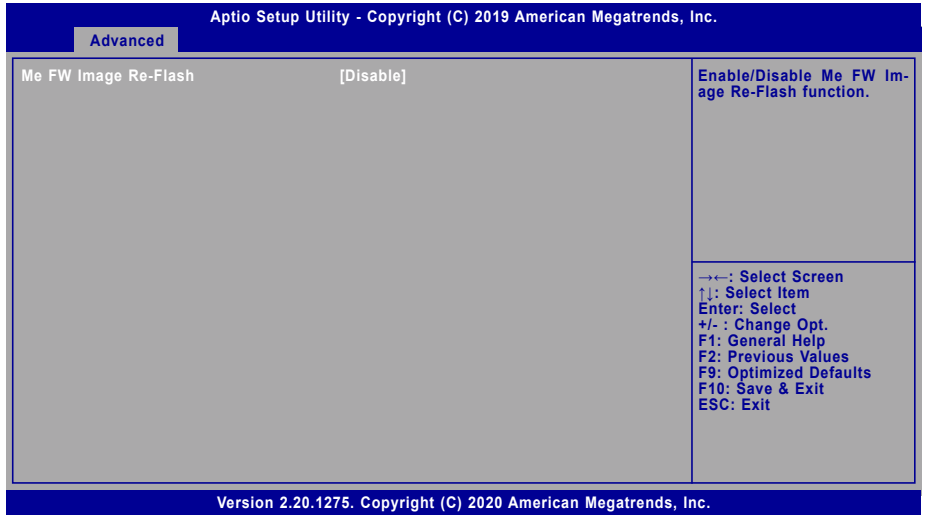
Hide Unconfigure ME Confirmation Prompt

Enable or disable to hide unconfigure ME confirmation prompt when attempting ME unconfiguration.

Unconfigure ME

Enable or disable to unconfigure ME with resetting MEBx password to default.

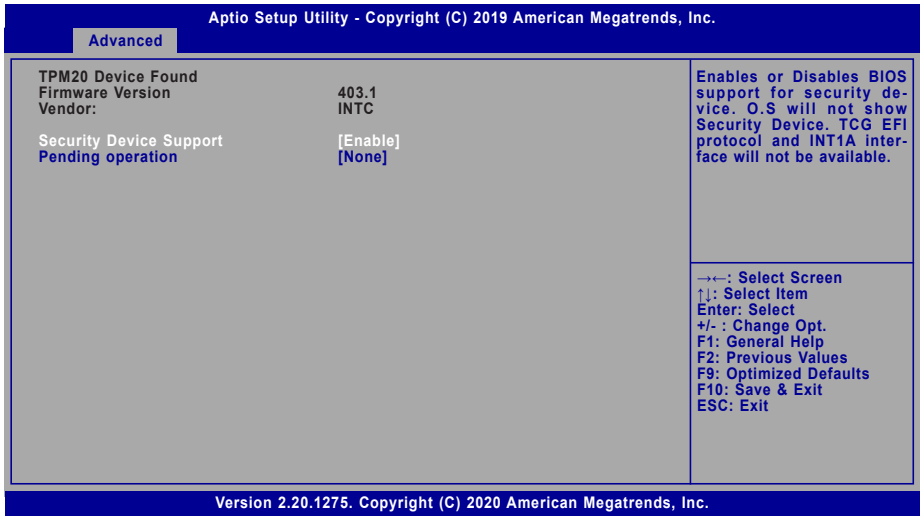
Fireware Update Confuguration



Me FW Image Re-Flash

This field is used to enable or disable the ME FW Image Re-Flash function, which allows the user to update the ME firmware.

Trusted Computing



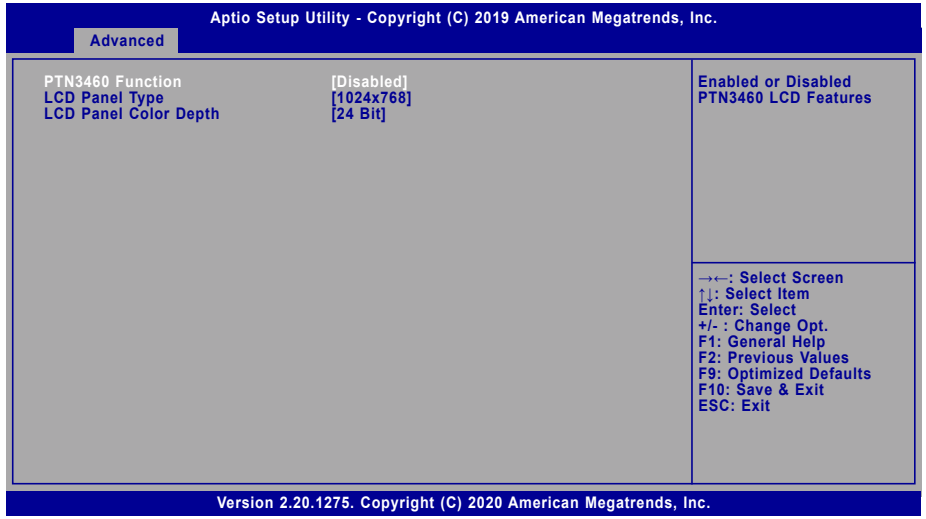
Security Device Support

This field is used to enable or disable BIOS support for the security device such as an TPM 2.0 to achieve hardware-level security via cryptographic keys.

Pending operation

To clear the existing TPM encryption, select "TPM Clear" and restart the system. This field is not available when "Security Device Support" is disabled.

PTN3460 Configuration



PTN3460 Function

Enable or disable PTN3460 LCD features. The following fields are only configurable when this field is enabled.

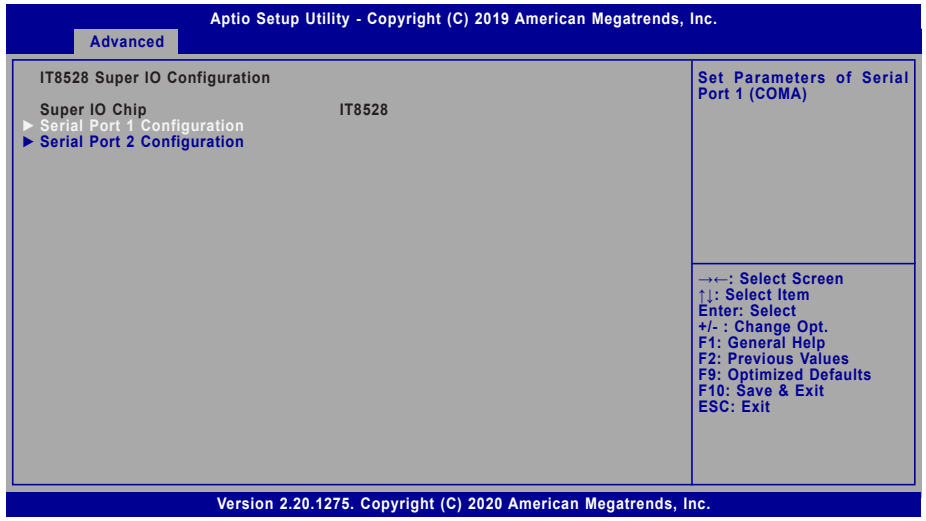
LCD Panel Type

Select the resolution of the LCD Panel — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1280X768, 1920X1080, or 1600X900.

LCD Panel Color Depth

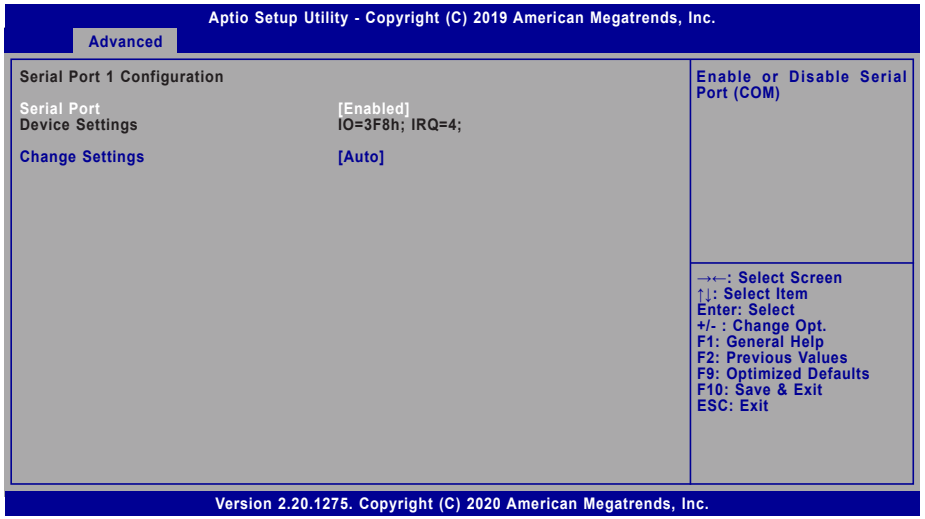
Select the color depth of the LCD Panel — 18 Bit, 24 Bit, 36 Bit, 48 Bit

IT8528 Super IO Configuration



Note:
The sub-menus are detailed in following sections.

IT8528 Super IO Configuration - Serial Port 1/2 Configuration



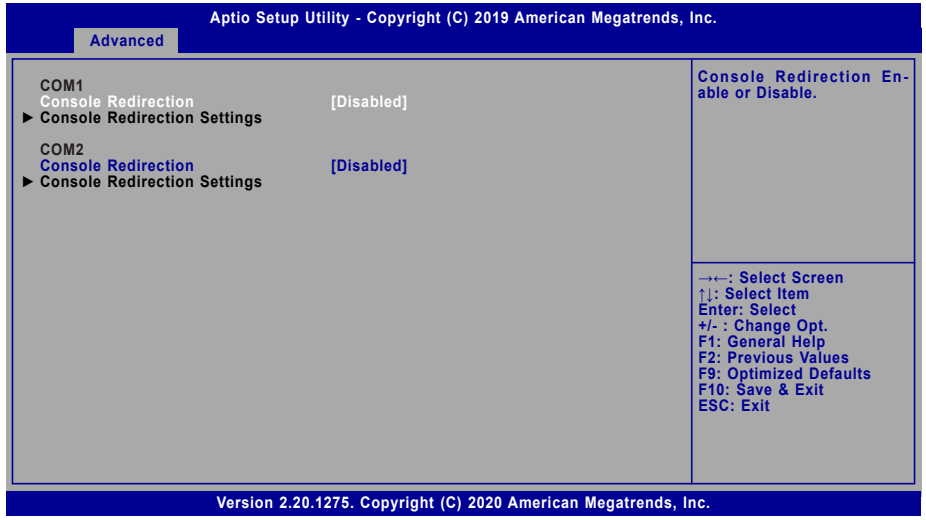
Serial Port

Enable or disable the current serial COM port.

Change Settings

Select an I/O Address and IRQ for the current serial Port, or select Auto to assign automatically.

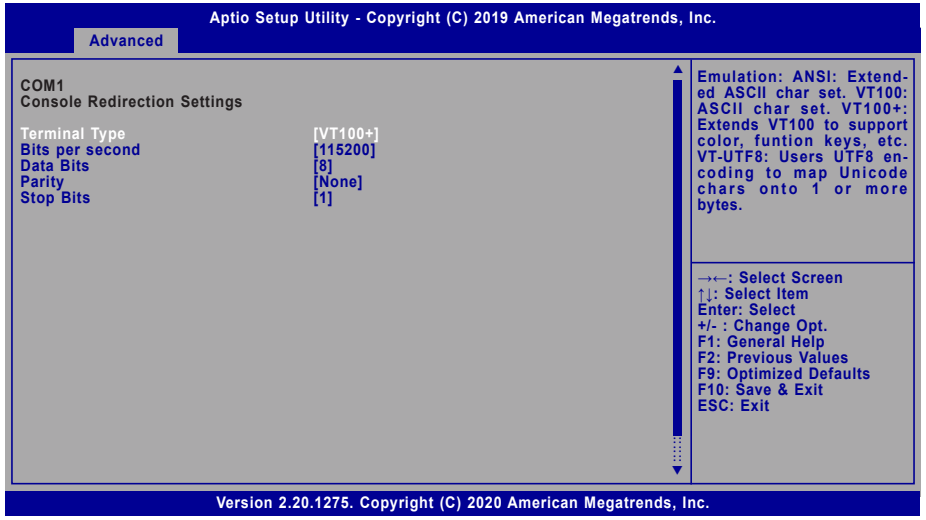
Serial Port Console Redirection



Console Redirection

By enabling Console Redirection of a COM port, the sub-menu of console redirection settings will become available for configuration as detailed in the following pages.

Console Redirection Settings



Configure the serial settings of the current COM port.

Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

Data Bits

Select data bits: 7 bits or 8 bits.

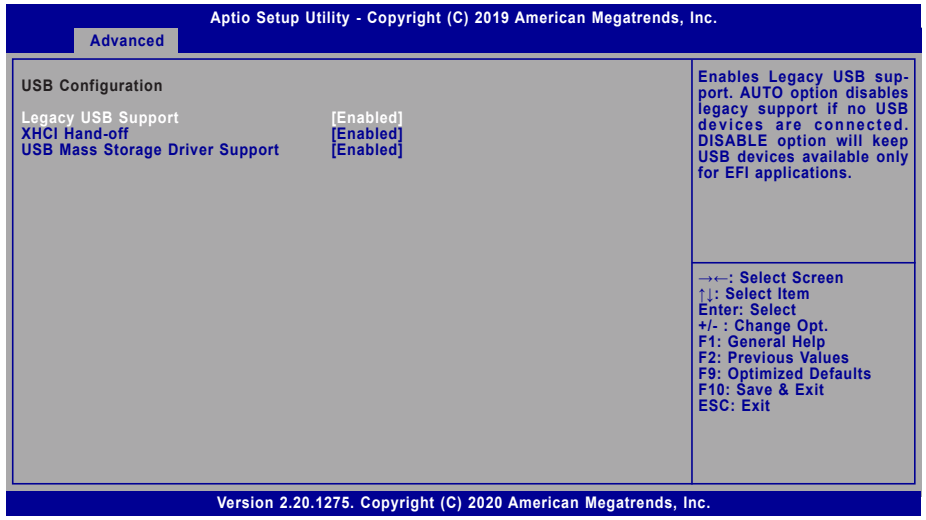
Parity

Select parity bits: None, Even, Odd, Mark or Space.

Stop Bits

Select stop bits: 1 bit or 2 bits.

USB Configuration



Legacy USB Support

Enabled Enable Legacy USB support.

Disabled Keep USB devices available only for EFI applications.

Auto Disable Legacy support if no USB devices are connected.

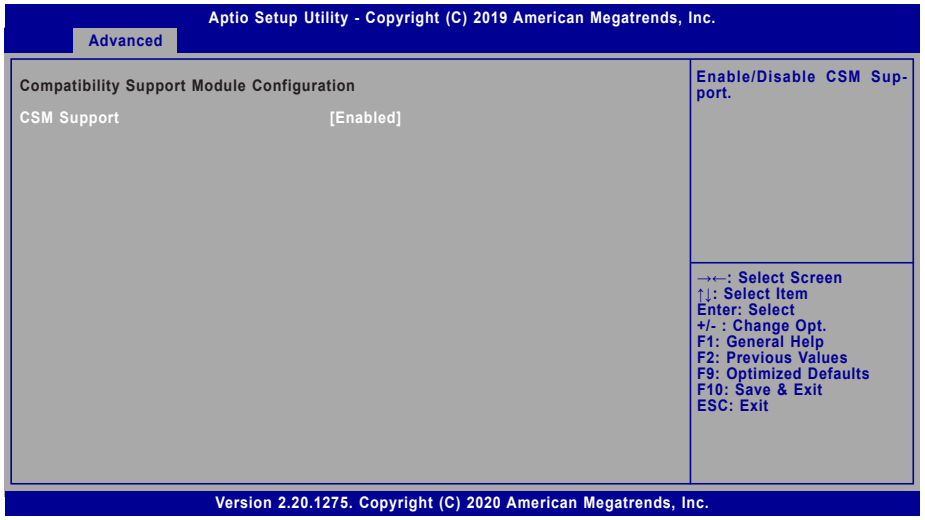
XHCI Hand-off

Enable or disable XHCI Hand-off.

USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

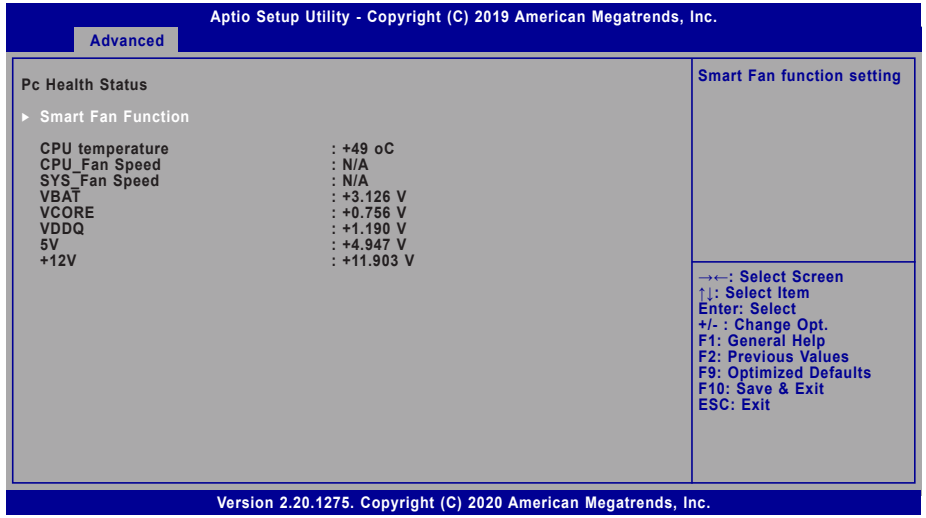
CSM Configuration



CSM Support

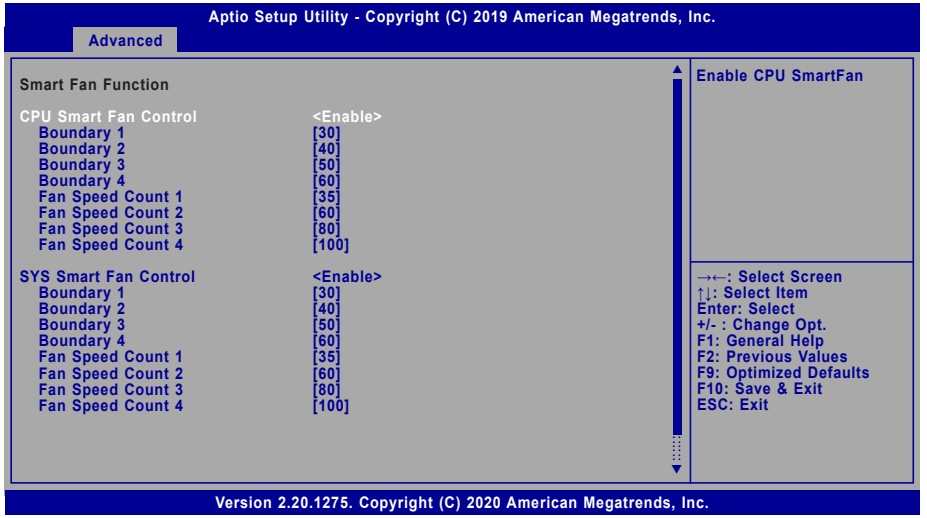
This section is used to enable or disable CSM Support. Fields in following pages are only available when "CSM Support" is enabled.

PC Health Status



This section displays the system's health information, i.e. voltage readings, CPU and system temperatures, and fan speed readings.

PC Health Status - Smart Fan Function



Smart Fan is a fan speed moderation strategy dependent on the current system temperature. When the system temperature goes higher than the Boundary setting, the fan speed will be turned up to the setting of the Fan Speed Count that bears the same index as the Boundary field.

▼ SYS Smart Fan/CPU Smart Fan Control = [Enabled]

Boundary 1 to Boundary 4

Set the boundary temperatures that determine the fan speeds accordingly, the value ranging from 0-127°C. For example, when the system temperature reaches Boundary 1 setting, the fan speed will be turned up to the designated speed of the Fan Speed Count 1 field.

Fan Speed Count 1 to Fan Speed Count 4

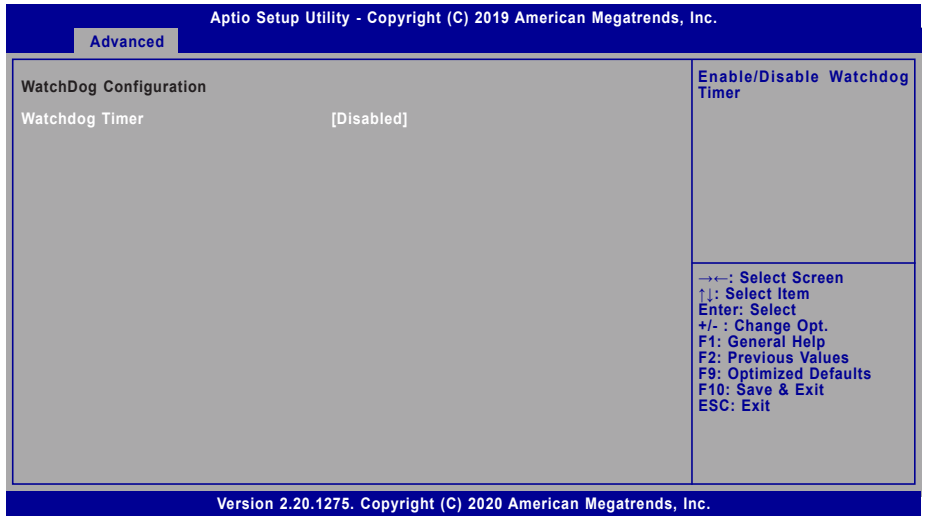
Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will operate according to the specified boundary temperatures above-mentioned.

▼ SYS Smart Fan/CPU Smart Fan Control = [Disabled]

Fix Fan Speed Count

Set the fan speed, the value ranging from 1-100%, 100% being full speed. The fans will always operate at the specified speed regardless of gauged temperatures.

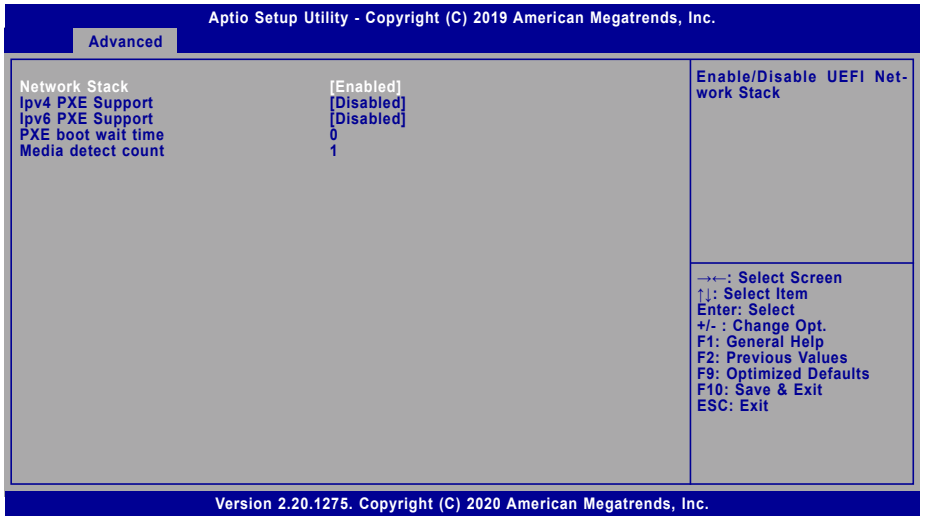
WatchDog Configuration



Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

Network Stack Configuration



Network Stack

Enable or disable UEFI network stack. The following fields will appear when this field is enabled.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

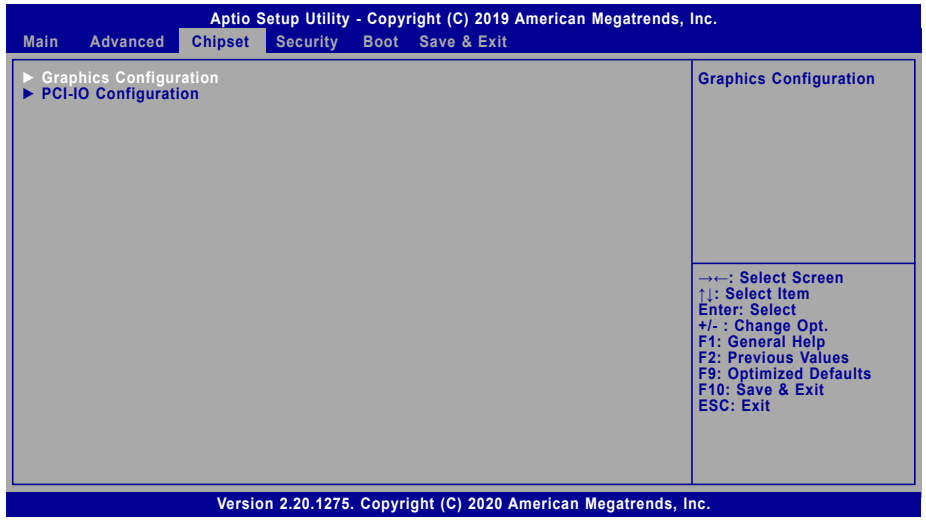
PXE boot wait time

Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

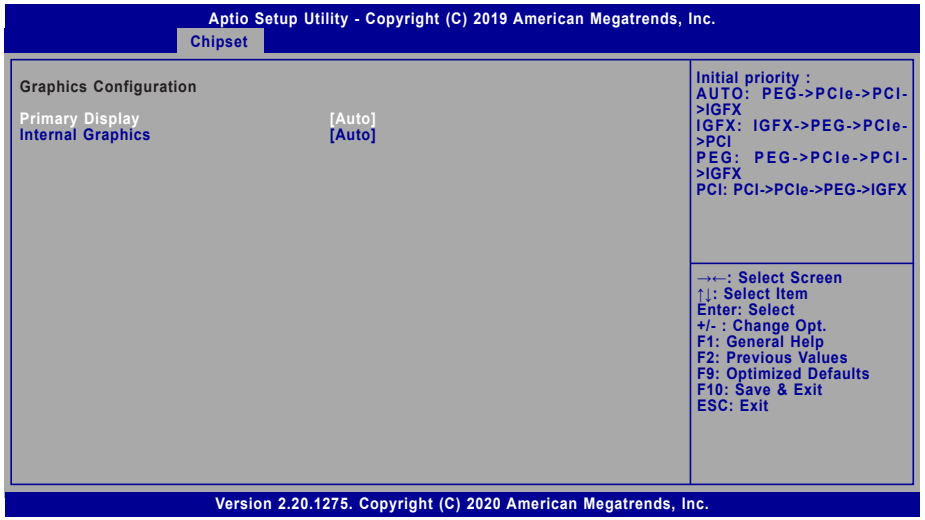
Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

Chipset



Note:
The sub-menus are detailed in following sections.

Graphics Configuration



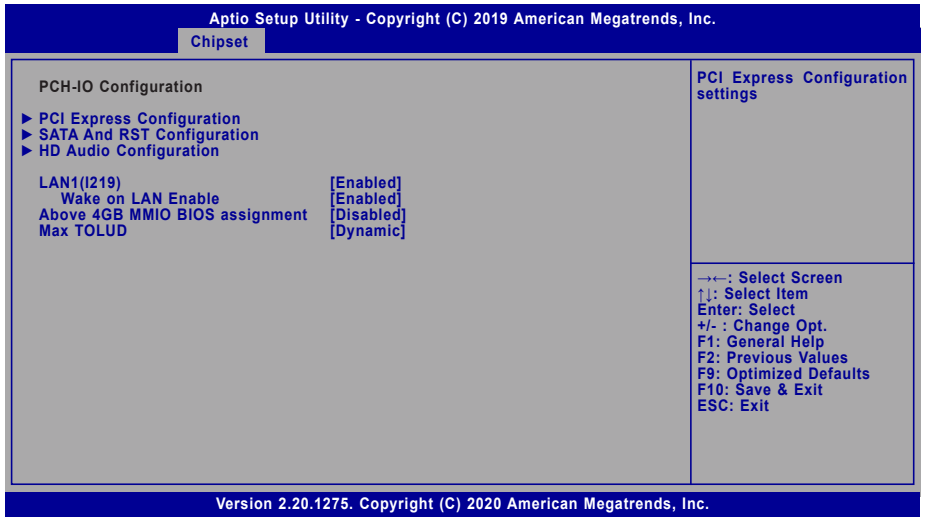
Primary Display

Select which of IGFX/PEG/PCI Graphics device to be the primary display.

Internal Graphics

Keep IGFX enabled based on the setup options.

PCH-10 Configuration



LAN1(I219)

Enable or disable onboard NIC.

Wake on LAN Enable

Enable or disable integrated LAN to wake the system.

Above 4GB MMIO BIOS assignment

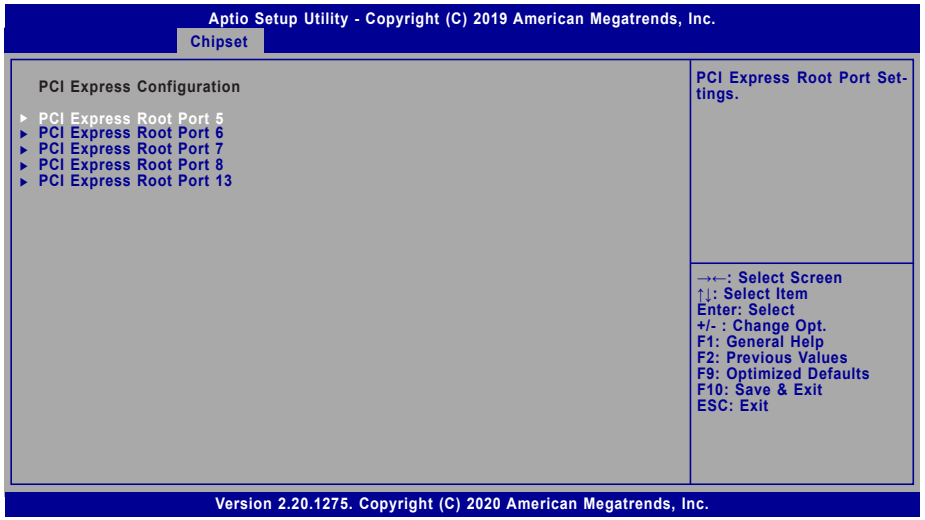
Switch MemoryMappedIO BIOS assignment above 4GB.

Max TOLUD

Assign a value or set "Dynamic" to automatically adjust TOLUD based on largest MMIO length.

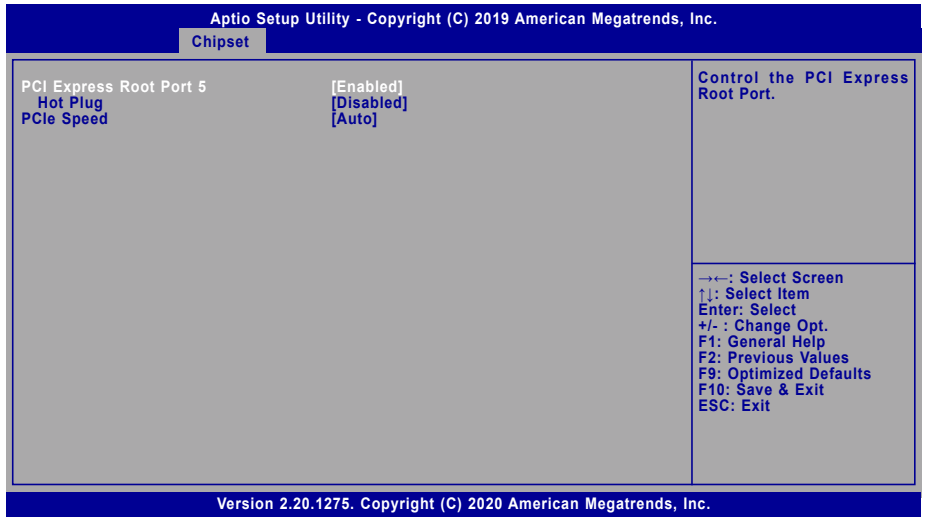
Note:
The sub-menus are detailed in following sections.

PCI Express Configuration



Note:
The sub-menus are detailed in following sections.

PCI Express Configuration - PCI Express Root Port 5/6/7/8/13



PCI Express Root Port 5/6/7/8/13

This field is used to enable or disable the PCI Express Root Port.

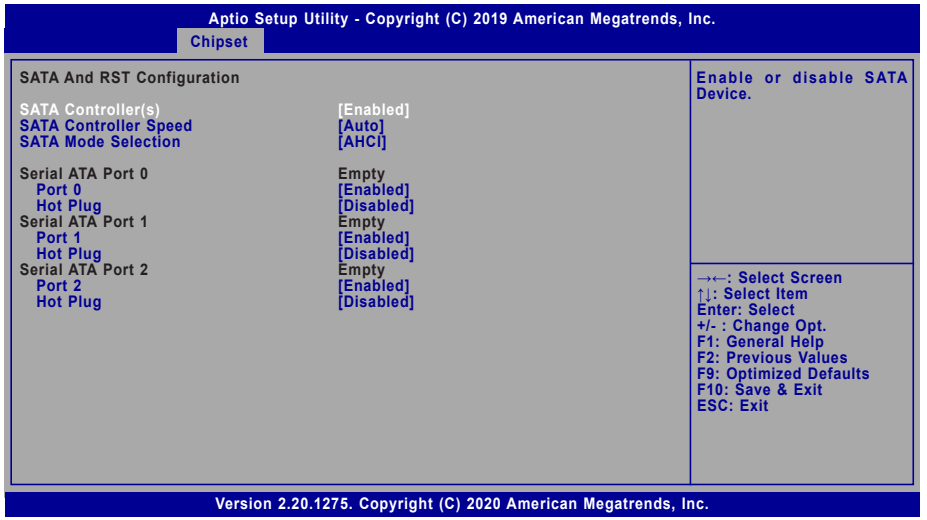
Hot Plug

This field is used to enable or disable the PCI Express Hot Plug.

PCIe Speed

Select the speed of the PCI Express Root Port: Auto, Gen1, Gen2 or Gen3.

SATA and RST Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Speed

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

AHCI This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

Intel RST Premium With Intel Optane System Acceleration This option allows you to create RAID or Intel Rapid Storage configuration along with Intel® Optane™ system acceleration on Serial ATA devices.

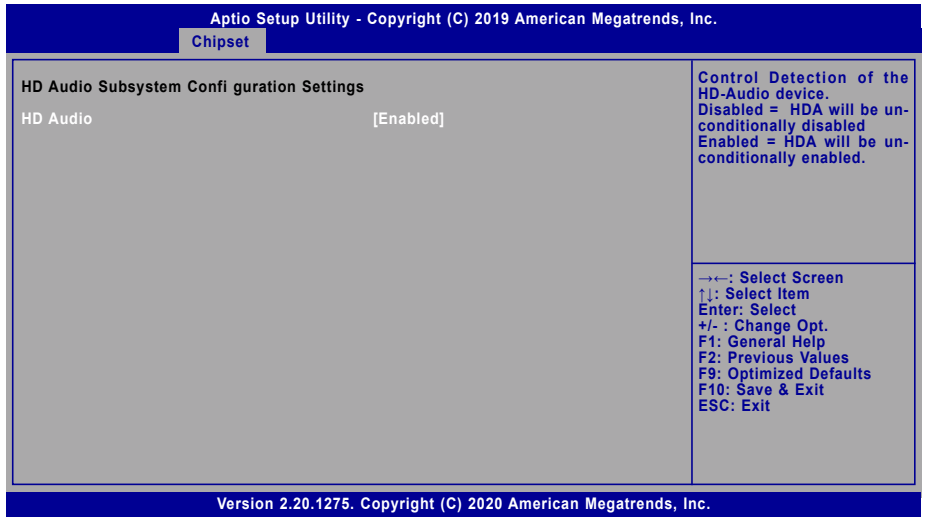
Use RST Legacy OROM

This field shows up when SATA Mode Selection is set to Intel RST Premium With Intel Optane System Acceleration. Enable or disable to use RST Legacy OROM when CSM is enabled.

Port 0/1/2 and Hot Plug

Enable or disable the Serial ATA port and its hot plug function.

HD Audio Configuration



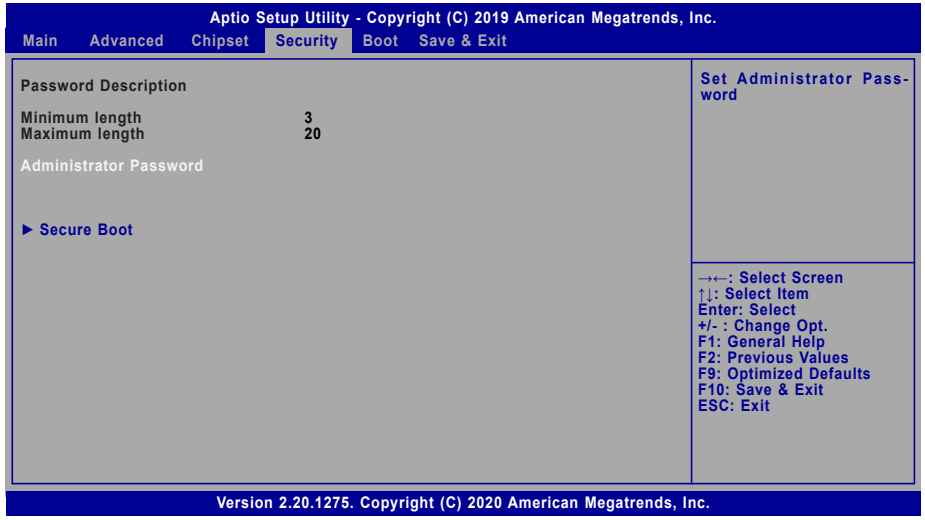
HD Audio

Control the detection of the HD Audio device.

Disabled HDA will be unconditionally disabled.

Enabled HDA will be unconditionally enabled.

Security



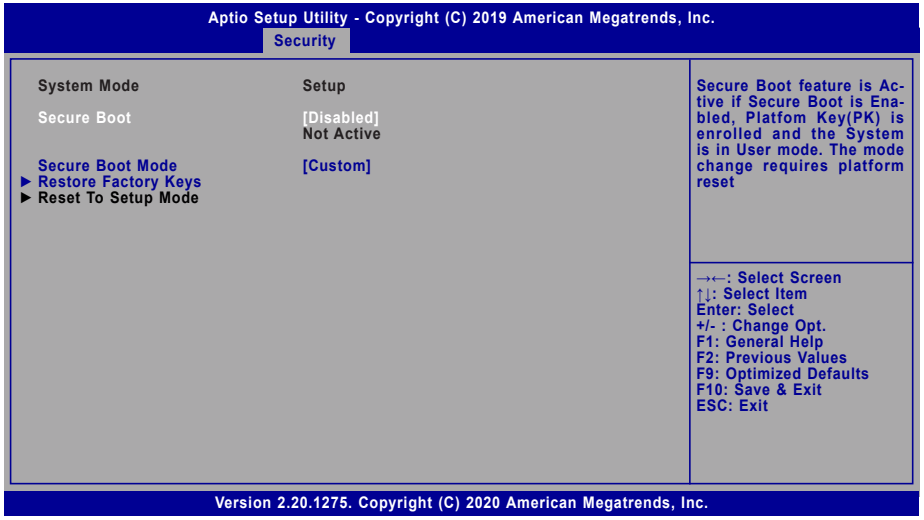
Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

User Password

Set the user password. To clear the password, input nothing and press enter when a new password is asked. User Password will be required when powering up the system.

Secure Boot



Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that "Secure Boot" is "[Enabled]", Platform Key (PK) is enrolled, "System Mode" is "User", and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be "Active".

Secure Boot Mode

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

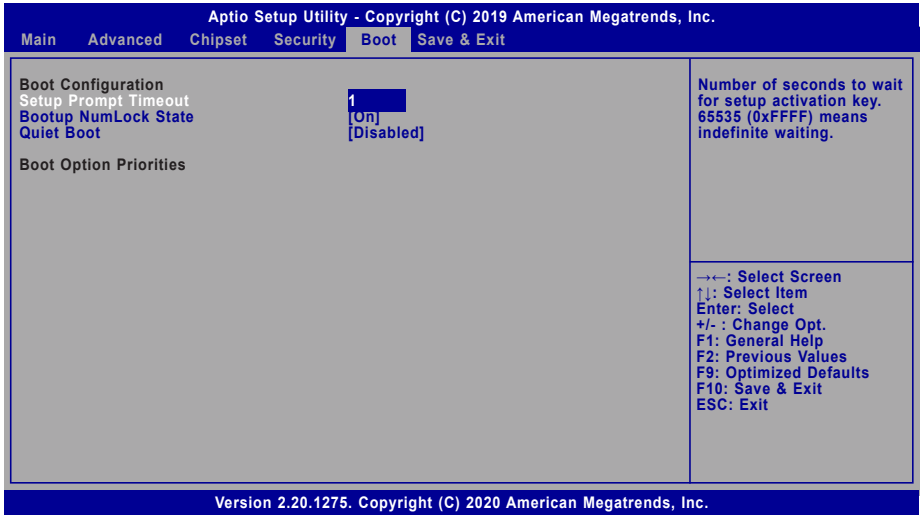
Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

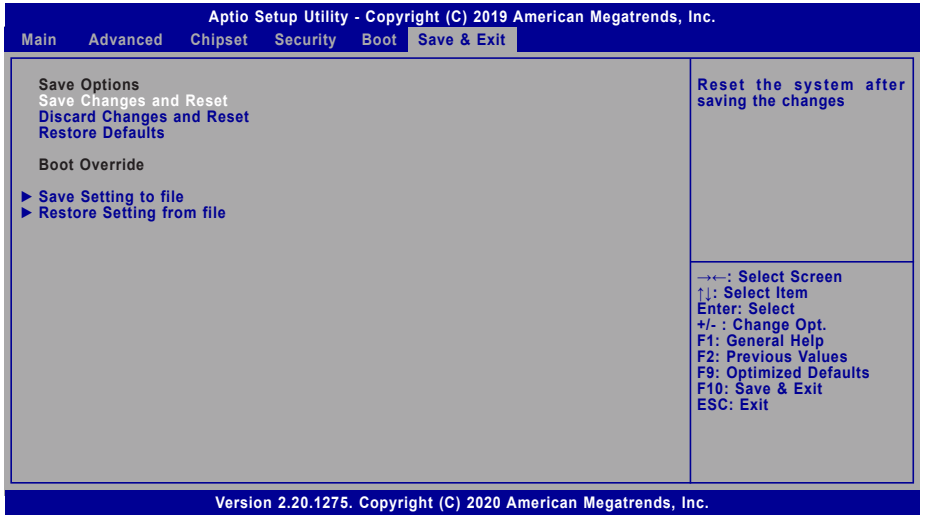
Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

Rearrange the system boot order of available boot devices.

Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The "Boot Option Priorities" configured in the Boot menu will not be changed.

► Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

► Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files. You may refer to how-to-video, How to update Insyde BIOS in UEFI mode on DFI products? Visit https://www.dfi.com/Knowledge/Video/31 for updating the BIOS steps.

Notice: BIOS SPI ROM

1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.